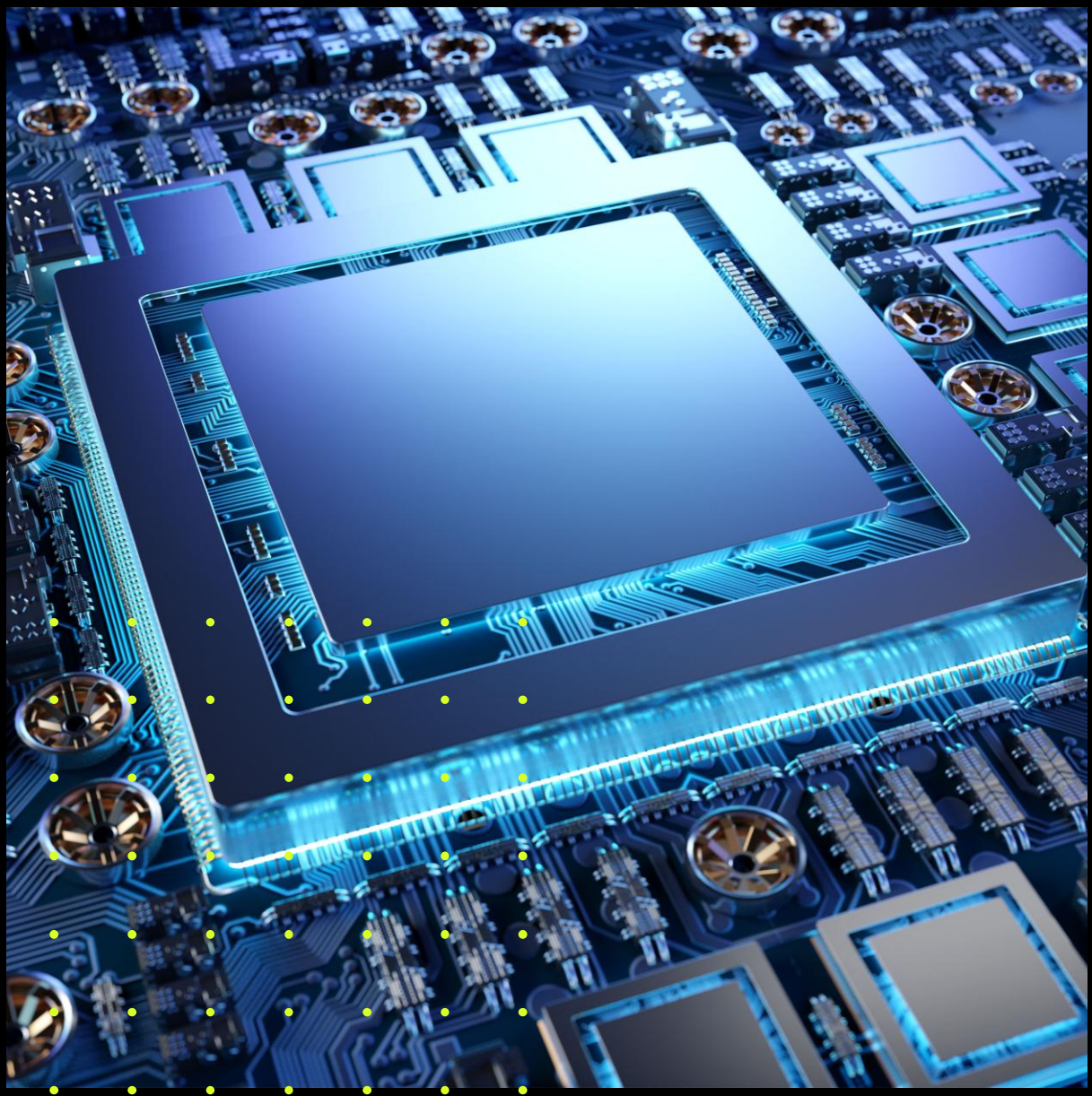

Architecting the Future: Building Smarter SoCs with RISC-V

How to balance performance, flexibility, and risk from concept to silicon

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Contents

This white paper is based on the Aion Silicon and Andes Technology webinar, "*Architecting the Future: Building Smarter SoCs with RISC-V.*" Watch the full session on YouTube.

1 Why Architecture Matters More Than Ever

For teams designing chips for AI, automotive, and high-performance edge systems, the question isn't if custom silicon is needed, but how to design it right the first time.

On advanced process nodes, even a so-called "prototype" tape-out can approach the cost of a full production mask set. A re-spin or a six-month slip isn't just inconvenient; it's a multi-million-dollar problem and often a missed market window. The cost of getting architecture wrong is now on the same order as the cost of the chip itself.

Architecture is where vision meets execution. It determines whether a chip will meet its targets, ship on schedule, and remain relevant as workloads evolve. It's also the only phase where you can still change fundamentals such as compute structure, memory hierarchy, and safety concepts without rewriting an entire design.

This white paper helps you:

- Understand how early architecture decisions drive both performance and commercial outcomes.
- Identify which trade-offs in power, performance, area, and flexibility actually move the needle.
- See how modeling and collaboration reduce the risk of re-spins on costly nodes.
- Understand how RISC-V's flexibility can be used intentionally, not impulsively.

> *"Right first silicon, meeting critical requirements, isn't simply an engineering aim. It's a commercial necessity."*
>
> **PAUL MARTIN**
> GLOBAL DIRECTOR OF SOC ARCHITECTURE
> **Aion Silicon**

2 From Requirements to Reality: Understanding the Architecture Process

Architecture is both a technical and a business discipline. Aion Silicon treats it as a structured program, not a single milestone. It begins with identifying what's essential, defining measurable targets, and aligning the design to commercial realities.

2.1 Must-Know Constraints Before You Begin

Category	What to Capture	Why It Matters
Performance & Power	Throughput, latency, and PPA targets	Establishes measurable KPIs
Interfaces & I/O	Bandwidths, signals, voltage levels	Determines architectural feasibility
Budget & Timeline	NRE limits, market window, tape-out goals	Connects architecture to business outcomes
Certification	FuSa, ISO 26262, or safety targets	Influences design structure and verification rigor
Software Ecosystem	Compiler, OS, and toolchain readiness	Impacts integration and time to validation

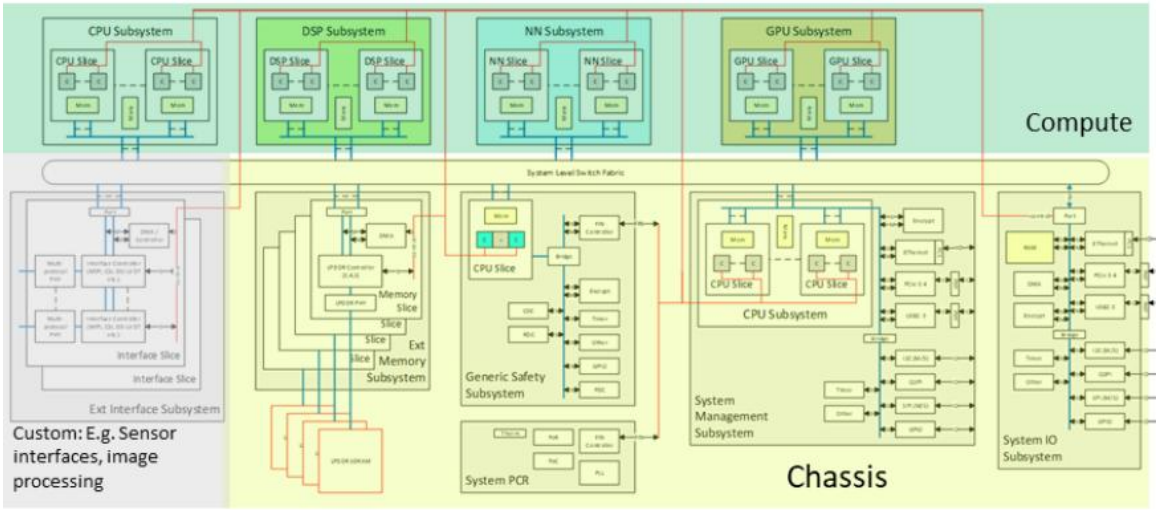
Once these are understood, Aion Silicon's process unfolds in four iterative stages:

1. Define requirements and use cases. Capture workloads and product goals.
2. Develop candidate architectures. Explore options within a scalable framework.
3. Model and validate. Simulate performance early to identify trade-offs.
4. Decide and document. Finalize the architecture spec and transition to RTL with confidence.

3 Making Trade-offs That Matter

Every SoC design is a balancing act. The real skill lies in recognizing which trade-offs deliver measurable benefit, and cutting the ones that only add complexity, verification risk, or cost. Each decision, from cache size to interconnect topology, carries ripple effects across performance, power, and safety targets. The architecture phase is where those trade-offs can still be modeled, tested, and decided with data instead of assumptions.

Aion Silicon's process treats this as a structured exercise, not guesswork. By modeling early and refining continuously, design teams can explore performance and cost envelopes before committing to RTL, choosing where to invest engineering effort and where to keep it simple.



Functions mapped onto a scalable, extensible architecture framework

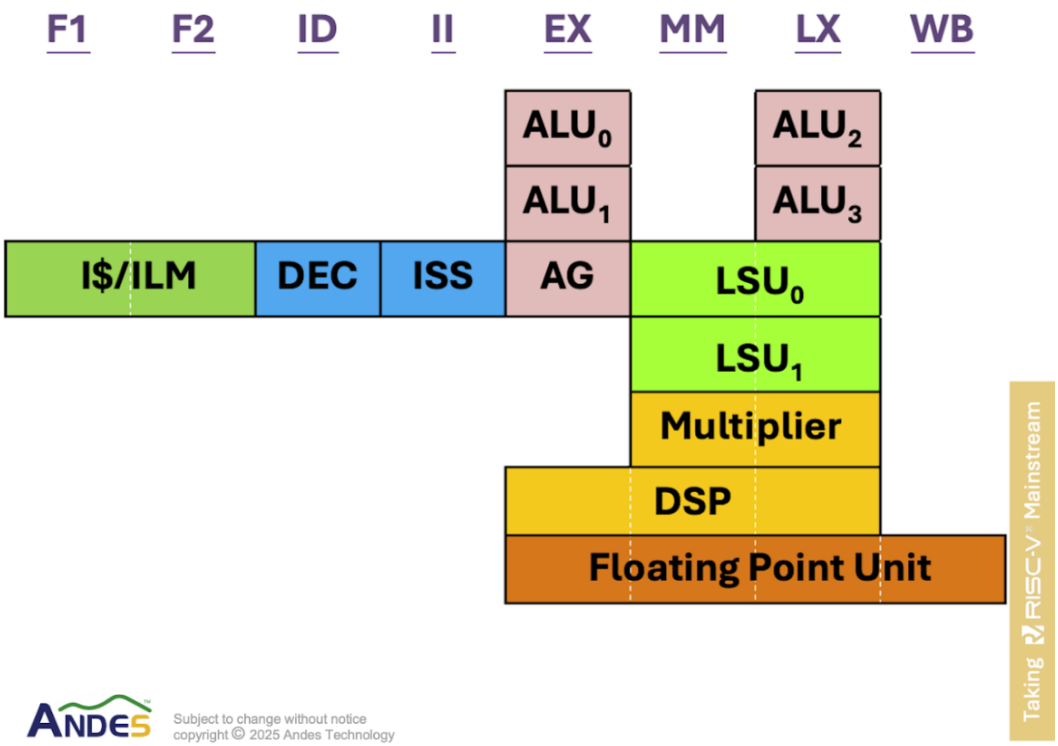
3.1 Aion Silicon's Scalable Framework

Layer	Purpose	Examples
Compute Subsystems	Processing elements tailored to workloads	CPUs, DSPs, Vector engines, GPUs
Chassis / Fabric Layer	Shared memory, interconnect, and system management	On-chip memory, clock and power control
Custom Logic & Peripherals	Application-specific acceleration	Sensor or imaging pipelines, signal processors
Safety & Security Subsystem	Functional safety and data protection	Lock-step cores, safety islands, root of trust

3.2 Processor Choices at a Glance

Processor Type	Core Characteristics	Ideal Workloads	Strength
CPU	Scalar, sequential instruction flow	OS, control code, general compute	Versatile and flexible
DSP	Specialized for streaming math	Audio, radar, sensor fusion	Low latency, low power
Vector Processor	SIMD operations on many data elements	Image processing, AI kernels	Efficient for numeric operations
GPU	Massively parallel threads	Graphics, ML inference or training	High throughput and scalability

While processor selection determines what a system can do, the internal pipeline determines how well it does it. The diagram below highlights the arithmetic, logic, load/store, DSP, and floating-point units that define the balance between throughput, latency, and energy use in a typical RISC-V core.



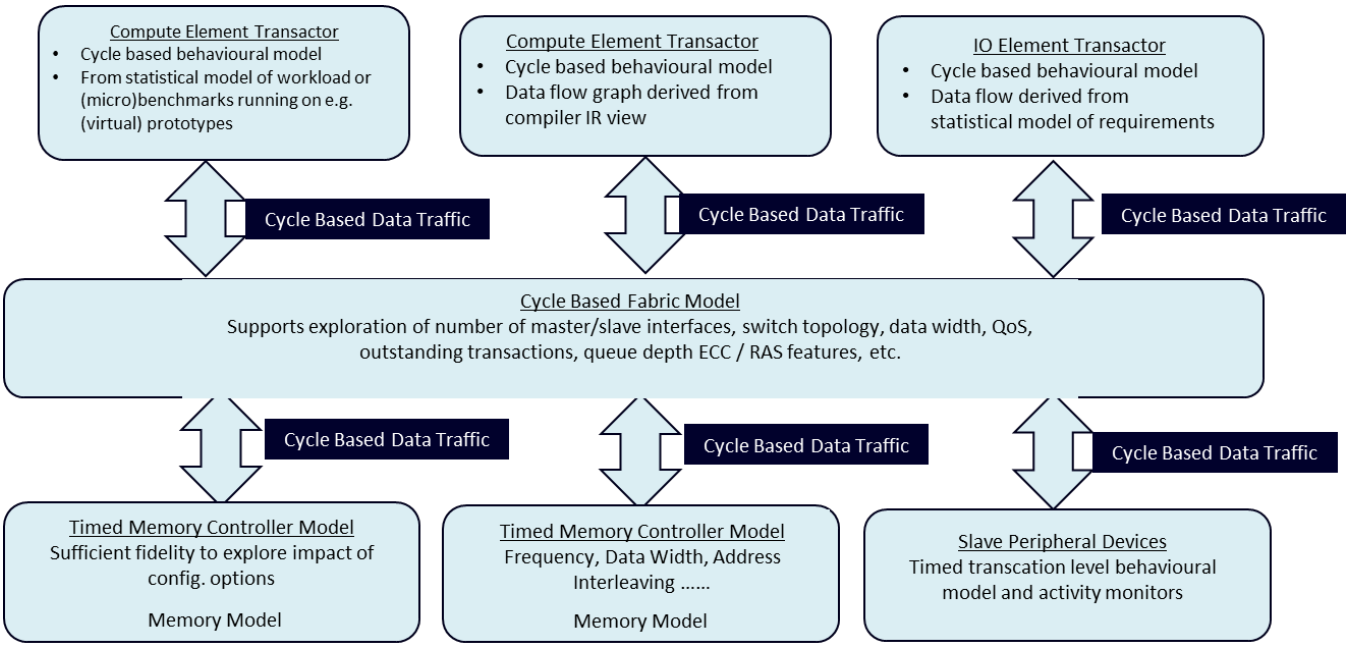
Simplified processor pipeline showing arithmetic, logic, load/store, DSP, and floating-point units, which are core elements influencing workload efficiency and power trade-offs.

4 Modeling, Simulation, and Optimization

Once the framework is set, modeling converts design intent into data. Using SystemC-based simulation, Aion Silicon builds cycle-accurate models of how workloads traverse the proposed architecture, testing throughput, latency, and memory efficiency before any RTL is written.

The goal is clear: prove that the design can meet its KPIs, under realistic traffic, while changes are still cheap. Modeling answers questions that spreadsheets and block diagrams can't: Where does contention actually occur? How sensitive is performance to cache size or bus arbitration? How much headroom do we really have?

4.1 Cycle-Based Modeling Flow



Aion Silicon's modeling environment connects compute, I/O, and memory subsystems through a cycle-based fabric model. Each component, including transactors, controllers, and peripherals, generates and consumes realistic data traffic to evaluate configuration options and bottlenecks before RTL.

4.2 Example: Modeling DNN Optimization

For AI workloads, Aion Silicon models the full neural network graph and use case directly in SystemC. The cycle-based simulation generates traffic profiles, fusion analysis, and node-reordering recommendations, all before RTL. This turns abstract model data into concrete architectural feedback on memory efficiency and throughput.

Input	Modeling Tool	Output
DNN graph + use case	SystemC cycle-based model	Traffic profiles, fusion analysis, node reordering recommendations

This closes the loop between architecture and performance tuning: every modeling iteration quantifies impact on KPIs like throughput and power efficiency.

Modeling Checklist:
✓ Confirm that active data sets fit in cache or on-chip memory.
✓ Quantify bus contention and memory access patterns.
✓ Correlate configuration changes directly to measurable KPI shifts.
✓ Use modeling results to prioritize fixes before RTL lock.

5 Collaboration and Program Alignment: Turning the Ecosystem into an Advantage

Datasheets don't deliver successful SoCs; coordination does. Even the best architecture can fail without timely, transparent alignment across IP suppliers, EDA vendors, foundries, and toolchain partners. In complex programs, a solid technical design is only half the equation; the other half is keeping every contributor on schedule, informed, and accountable.

Aion Silicon approaches ecosystem management the same way it approaches architecture: structured, data-driven, and proactive. During the architecture phase, the team evaluates IP not just for technical fit, but for responsiveness, model maturity, and long-term reliability. Benchmark data, configuration models, and version tracking are aligned before verification begins, so downstream teams start with validated inputs instead of assumptions.

> *"Whether you're choosing cores, toolchains, or test benches, collaboration beats specification. Talk early, while changes are still possible."*

DARREN JONES
DISTINGUISHED ENGINEER & SOLUTIONS ARCHITECT
Andes Technology

This program-level discipline extends beyond IP. Aion Silicon maintains regular communication with every ecosystem partner, including foundries, OSATs, and EDA providers, to ensure design assumptions match real-world capabilities. When supply chain conditions or tool versions shift, issues are surfaced and resolved early, before they turn into schedule slips.

> *"We need reliable support. It's not a question of if something goes wrong, but when. The difference between a short delay and a six-month slip is the partner's ability to respond."*

PAUL MARTIN
Aion Silicon

Early collaboration also enables customization at lower cost. RISC-V lets teams add application-specific extensions, but this only works when architecture, verification, and IP partners plan for those changes up front. Andes Technology and Aion Silicon coordinate these extensions during architecture modeling, turning potential risks into controlled enhancements.

Programmatically, that's the difference between coordination and rework. What starts as a partnership on paper becomes a managed ecosystem, one that accelerates delivery instead of slowing it down.

6 RISC-V and the Discipline of Customization

RISC-V goes beyond processor selection; it changes how the entire architecture is planned and validated. Its open, modular ISA gives design teams the freedom to shape their compute architecture precisely to each workload, from dense AI inference to safety-critical automotive control. That freedom also raises the stakes: every extension ripples through the core, memory system, toolchain, and verification plan. Without structure, customization adds cost instead of value.

6.1 Aion Silicon's methodology keeps that flexibility disciplined and predictable.

Customization with purpose.
RISC-V lets designers add custom instructions that make silicon more efficient for a given use case. At Aion Silicon, each extension is tied to a defined workload and validated through modeling, not instinct. The goal is measurable gain, not novelty. Even configuring a floating-point unit for 32-bit instead of 64-bit precision can halve area and power when planned early.

Early, joint planning.
Many RISC-V projects require one or two architectural tweaks to make custom IP "fly." That's where collaboration matters. Aion Silicon and Andes coordinate during the architecture phase to decide what to configure, what to extend, and what to leave standard. This alignment avoids the six-month schedule slips that can come from waiting on missing updates or late-stage support.

Rigorous validation through modeling.
Each customization is modeled and simulated in SystemC to quantify its impact on throughput, latency, power, and safety targets before RTL. By combining Andes's RISC-V IP expertise with Aion Silicon's system-integration and modeling strengths, customers gain data-driven confidence that new instructions and micro-architectural changes deliver the intended performance and remain certifiable.

This makes RISC-V flexibility manageable: custom features are designed with data, validated before RTL, and delivered as part of a stable, system-ready architecture.

> *"Engage early and often with your IP providers. Decide what you need, and if you must design something yourself, figure that out as early as possible. Treat your IP providers as partners, because they want you to succeed."*
>
> **DARREN JONES**
> *Andes Technology*

7 The Takeaway: From Concept to Silicon

The most successful SoC teams share a few traits: they define early, model continuously, and collaborate across the entire ecosystem. They treat architecture as a measurable phase rather than a sketch on the way to RTL, and they make decisions with data rather than assumptions.

At Aion Silicon, that discipline drives every engagement. Each architecture is grounded in real workloads, simulated to eliminate blind spots, and aligned with partners whose roadmaps match the project's goals. The result is predictable innovation, silicon that performs as intended and arrives when the market is ready.

Architecture discipline comes down to a few consistent habits:

- Model early, decide deliberately. Bottlenecks are cheapest to fix before RTL.
- Build relationships before you need them. Ecosystem trust accelerates everything else.
- Customize with purpose. RISC-V's openness works best under architectural control.

> *"Architecture is a critical project in its own right, one that determines whether you hit your targets or spend the next year recovering."*
>
> **PAUL MARTIN**
> *Aion Silicon*

Architecture isn't a phase to finish, it's a foundation to build on. From first concept to proven silicon, the right structure, partners, and modeling approach make all the difference.

8 About Aion Silicon

Founded in 2002, **Aion Silicon** is the trusted partner of choice for handling every stage of an IC's creation. Its award-winning, define and design ASIC consulting capability is fully complemented by its turnkey ASIC manufacturing services to transform designs into tested, volume-packaged silicon chips. This single point of contact for the entire supply chain process ensures low risk and faster times to market. Headquartered in the UK, Aion Silicon supports customers around the world via its offices in India, Spain, Morocco and North America.

For more information, visit www.aionsilicon.com

This eBook was produced in collaboration with Andes Technology, a leading provider of RISC-V processor IP.