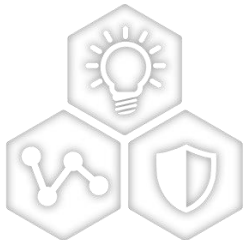


Creating High-Performance Cool Running Edge Nodes



A Leading Provider of Smart, Connected and Secure Embedded Control Solutions



SMART | CONNECTED | SECURE

FPGA

Agenda

- **System cost of power consumption in all applications**
- **Benefits of lower power consumption**
- **Example applications**
- **Demonstration**

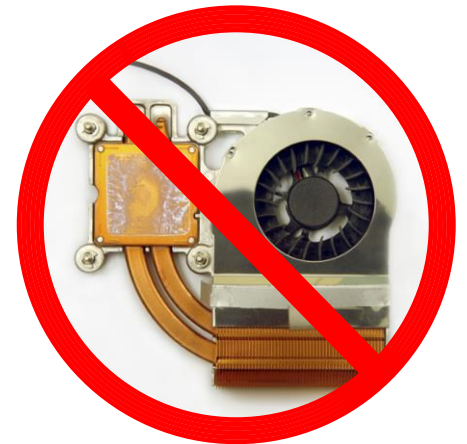
Why Power Consumption Matters

System Implications

Why Power Consumption Matters

Important for all Applications

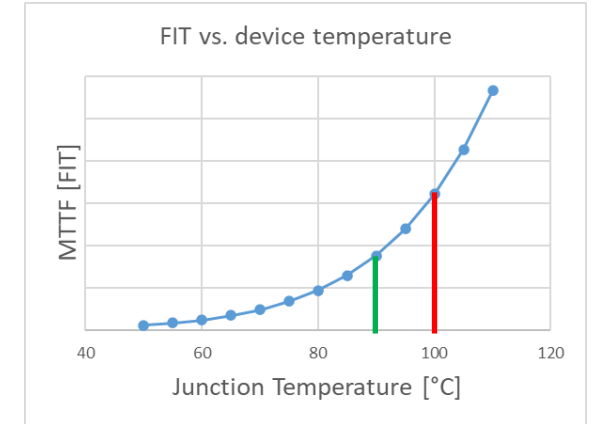
- **Power consumption is far beyond “battery-life”**
 - Lower power = lower self heating
 - **No heat sinks or fans**
 - Avoids cost and components that can fail
 - Smaller physical system size and lower system cost
 - Longer device lifetime due to lower junction temperature
 - Longer mean time to failure (MTTF) = lower failure in time (FIT)-rate
 - More features on power budget
- **Big 3**
 - Reduce risk
 - Save money
 - Make money



Reliability and Power

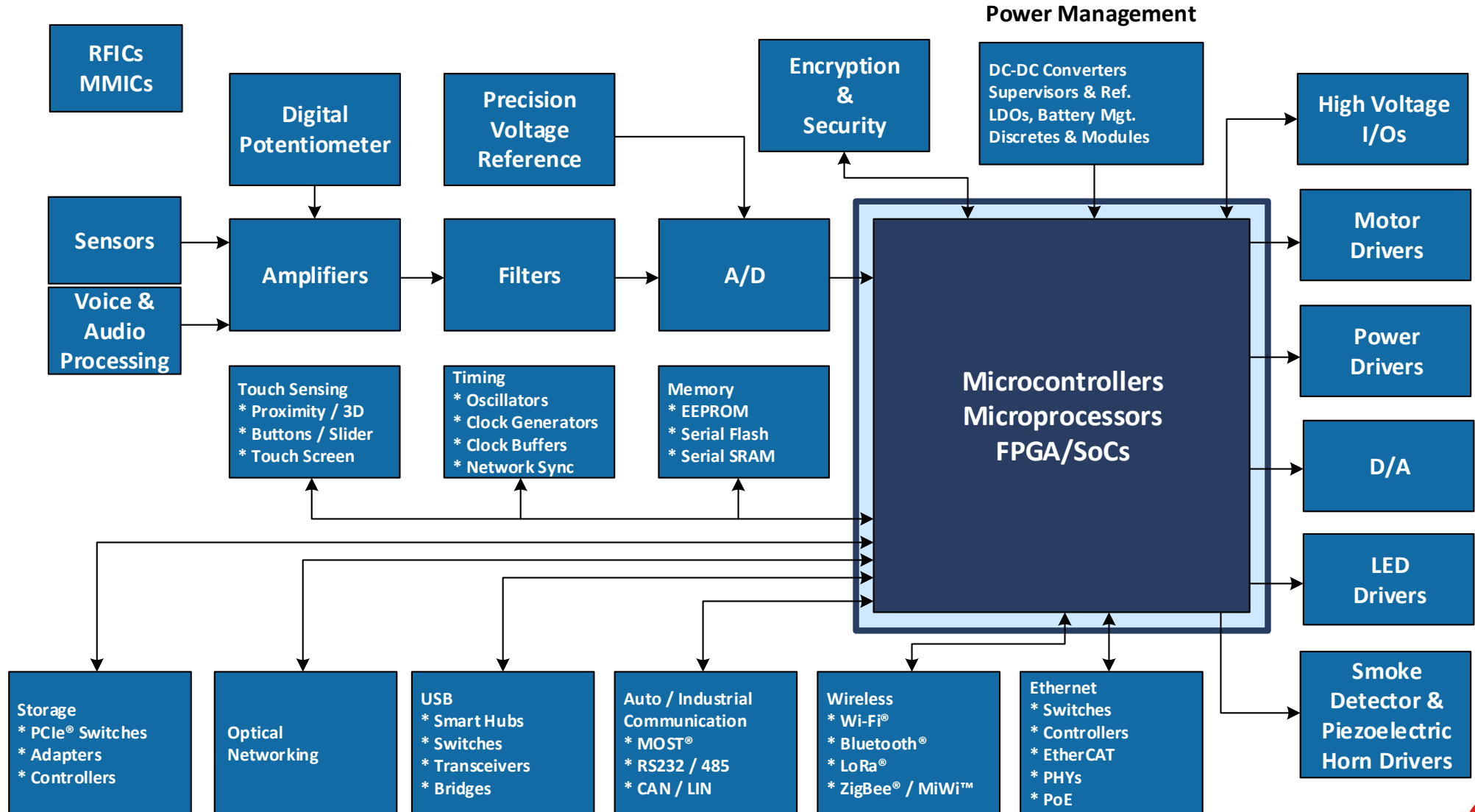
Why Power Matters for Reliability

- **Reliability cares about failure rates**
 - Measured in Failure In Time (FIT)
 - FIT-rate is strongly dependent on temperature
 - Decreasing the device-temperature by 10°C approximately halves the FIT-rate
- **Higher FIT in hardware = harder for safety certification**



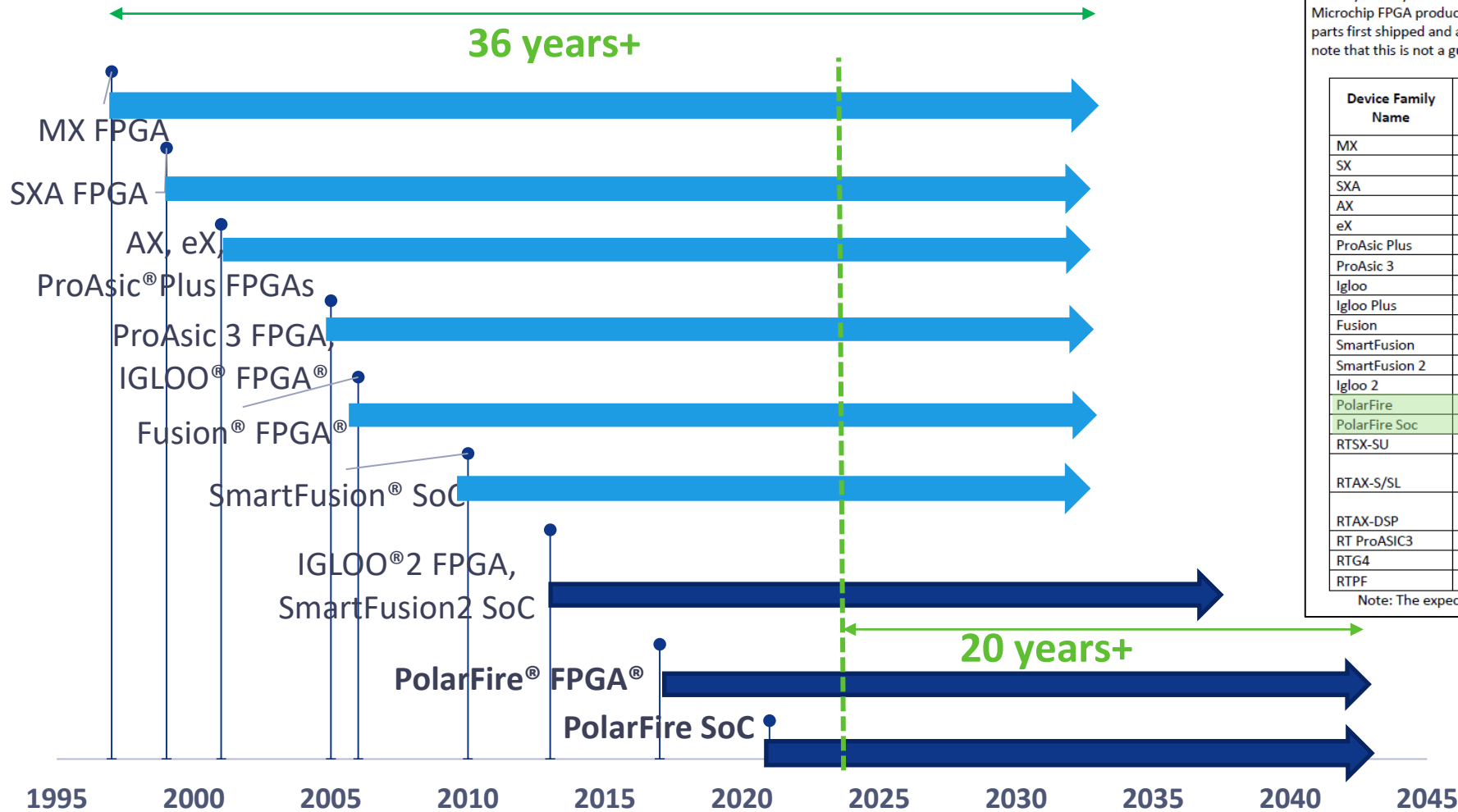
Providing Full System Solutions

Portfolio of Hardware, Software and Services



Microchip No Obsolescence Practice

Longevity of Supply



Note: Longevity timelines show historic and anticipated years of support. Some external factors could impact the timelines.

March 10, 2023

Dear Valued Customer,

Thank you for your continued interest in Microchip products. The purpose of this letter is to address Microchip FPGA product longevity. Below you will find a matrix of device families with data on when parts first shipped and an approximate timeframe that we expect to have wafer availability; please note that this is not a guarantee of availability.

Device Family Name	Microsemi Part Number Starts With...	Year First Shipped	Expected Availability from 2023
MX	A40MX, A42MX	1997	10 years
SX	A54SX	1999	5 years
SXA	A54SX_A	1999	10 years
AX	AX	2001	10 years
eX	eX	2001	10 years
ProAsic Plus	APA	2001	10 years
ProAsic 3	A3P, A3PN, A3PL	2005	10 years
Igloo	AGL, AGLN	2005	10 years
Igloo Plus	AGLP	2005	10 years
Fusion	AFS	2006	10 years
SmartFusion	A2F	2010	10 years
SmartFusion 2	M2S	2013	15 years
Igloo 2	M2GL	2013	15 years
PolarFire	MPF	2017	20 years
PolarFire Soc	MPFS	2021	20 years
RTSX-SU	RTSXxxSU	2004	10 years
RTAX-S/SL	RTAXxxxS, RTAXxxxSL	2004	15 years
RTAX-DSP	RTAXxxxD, RTAXxxxDL	2011	15 years
RT ProASIC3	RT3P	2010	15 years
RTG4	RT4G150	2015	15 years
RTPF	RTPF	2022	20 years

Note: The expected supply continuity does not apply to EOL'ed products.

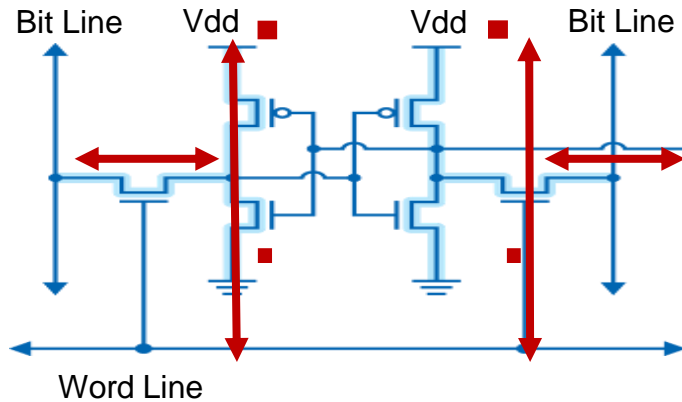
Power Efficiency

Architecture and Technology Matter

Significantly Lower Power Consumption

By Technology and by Design

SRAM Cell



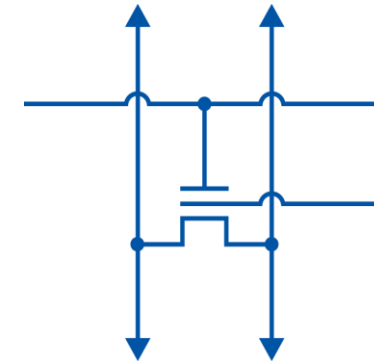
SRAM:

- Must continually re-charge
- Substantial leakage per cell

Features:

- Designed for HIGH-END market (and re-used for mid-range families)

Non-Volatile Cell



Non-Volatile memory:

- Retains its state
- 1000x lower leakage per cell

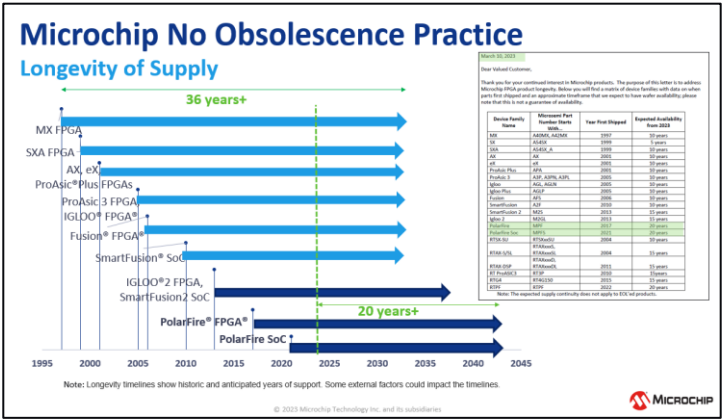
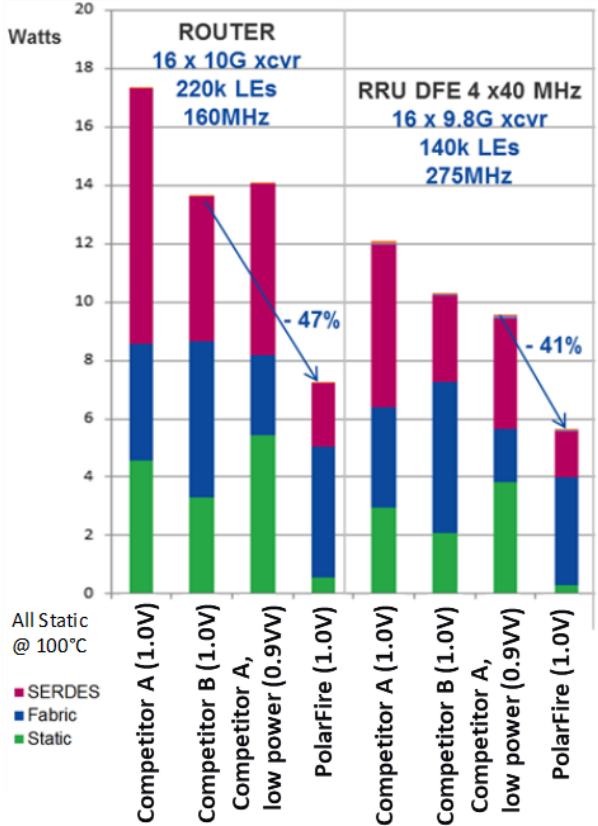
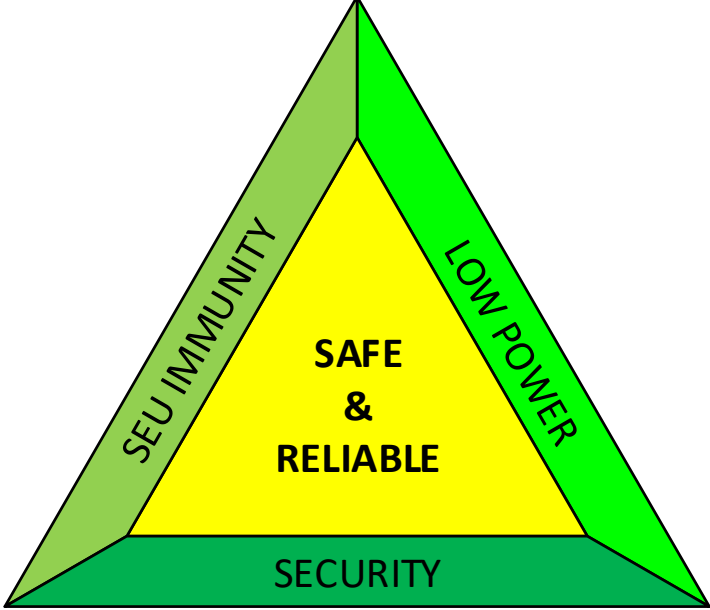
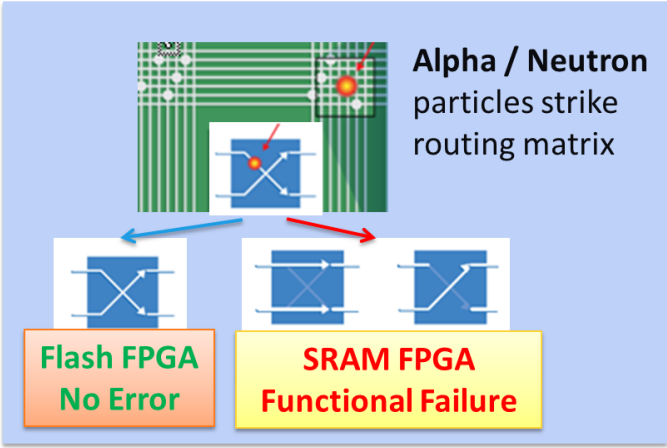
Features:

- Designed for LOW POWER (Transceivers, Microprocessors, etc.)

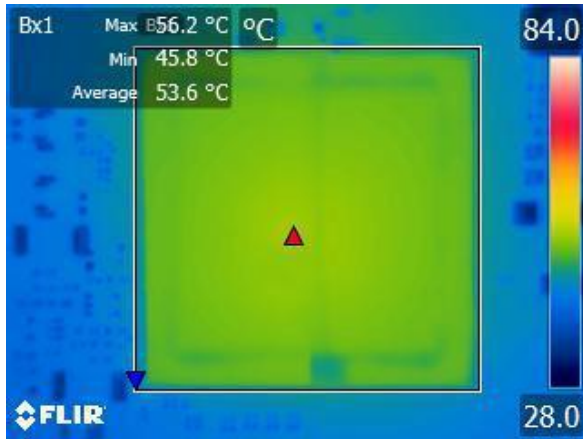
Total Power Savings of 30-50% vs SRAM FPGAs

Industrial as Multi-Faceted Topic

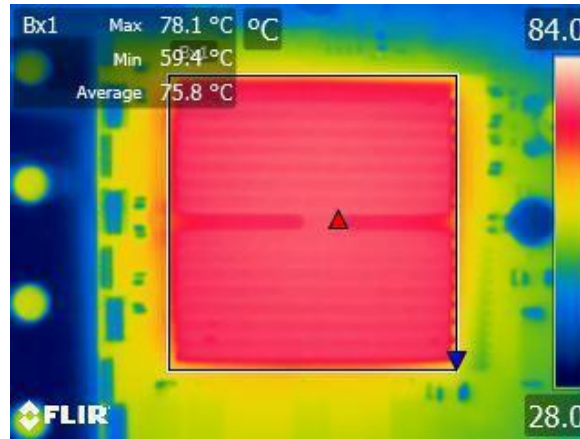
Microchip Key Items Support Industrial Applications



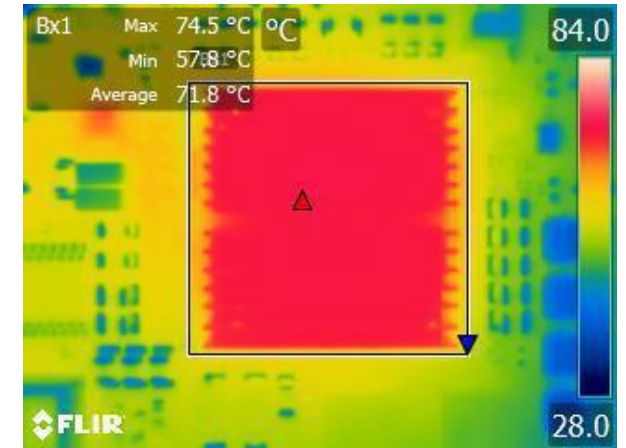
Significant Difference in Self-Heating



PolarFire® FPGA

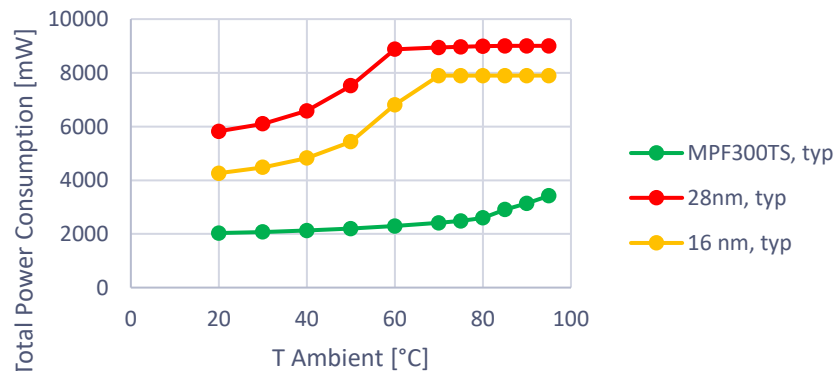


28 nm Competitor

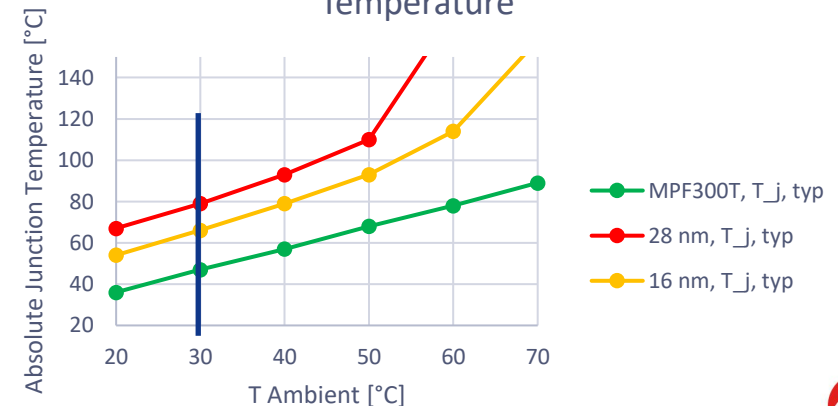


16 nm Competitor

Power Consumption vs. Ambient Temperature



Absolute Temperature vs. Ambient Temperature



Aging Caused by Temperature

What are Implications for the System?

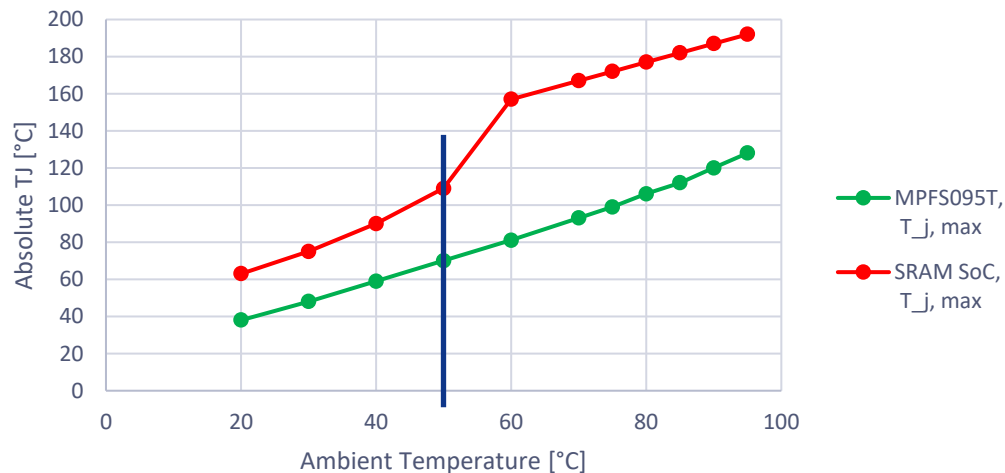
- **Device aging**

- $T_{\text{ambient}} = 50^{\circ}\text{C}$
- Junction temperature
 - PolarFire® SoC: **70°C**
 - SRAM SoC: **109°C**

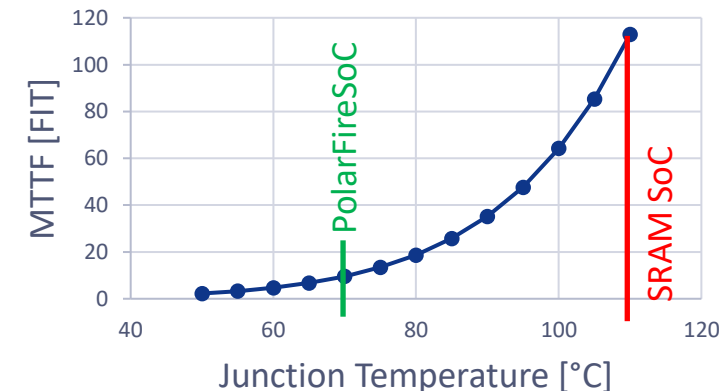
- **Resulting MTTF (assumed on identical test-hours)**

- PolarFire SoC: ~10 FIT
- SRAM SoC: ~107 FIT

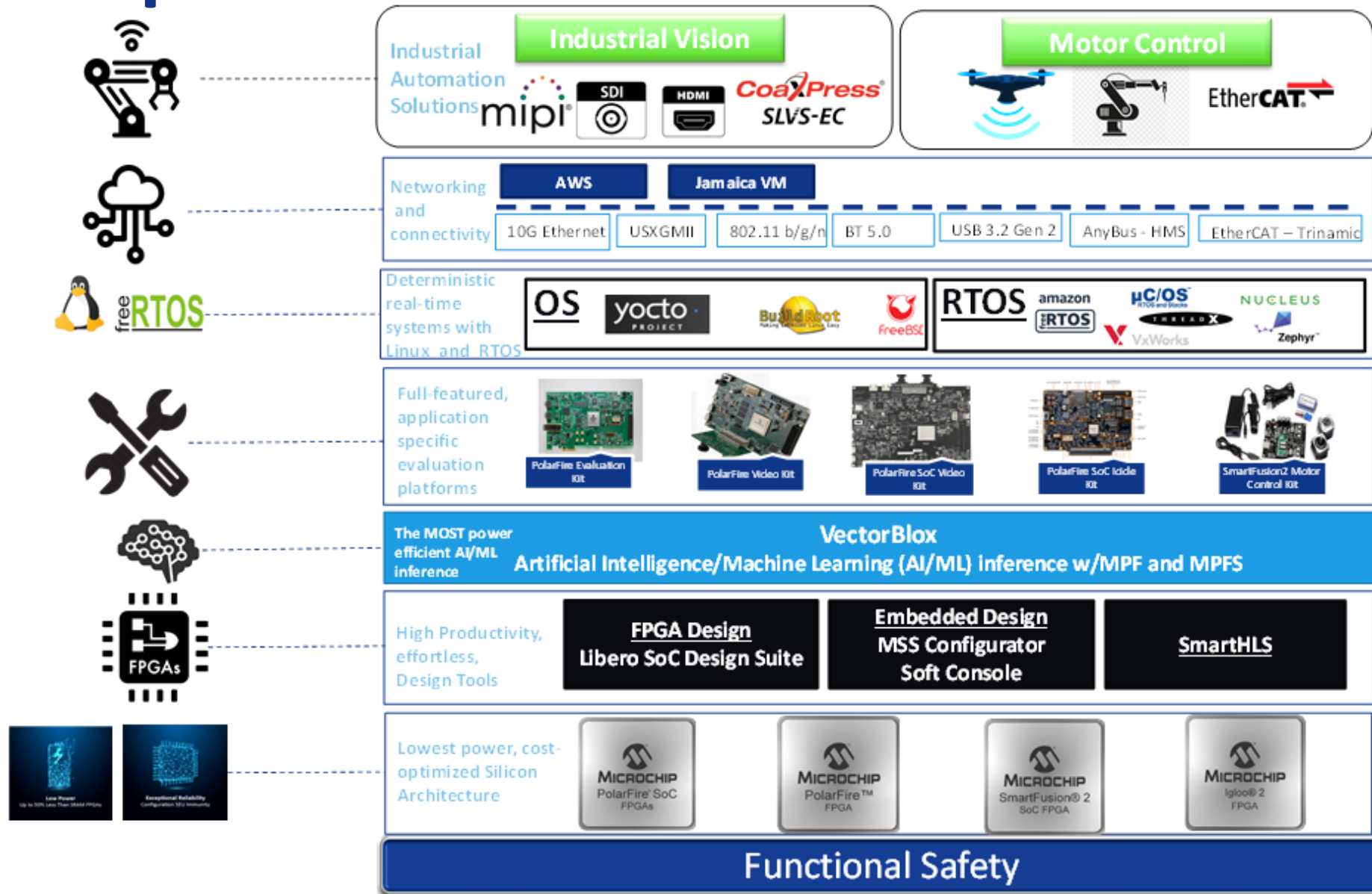
Absolute Temperature vs. Ambient Temperature



FIT vs. device temperature



Microchip Industrial Automation Stack



Hardware, Design and Data Security

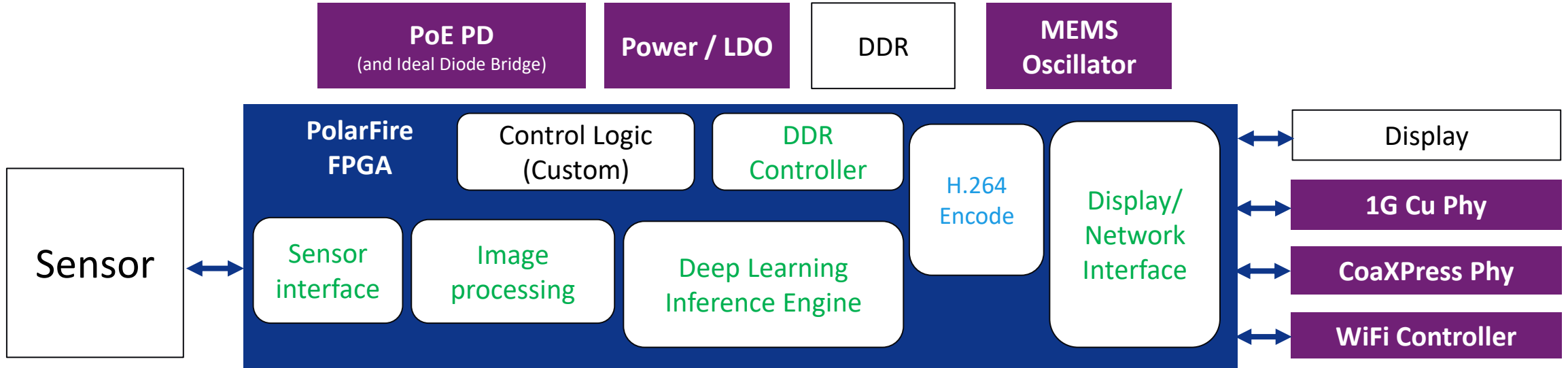


Example Applications

Key Element: Performance/Watt

High-Performance Industrial Camera

Optimizing for Performance/Watt



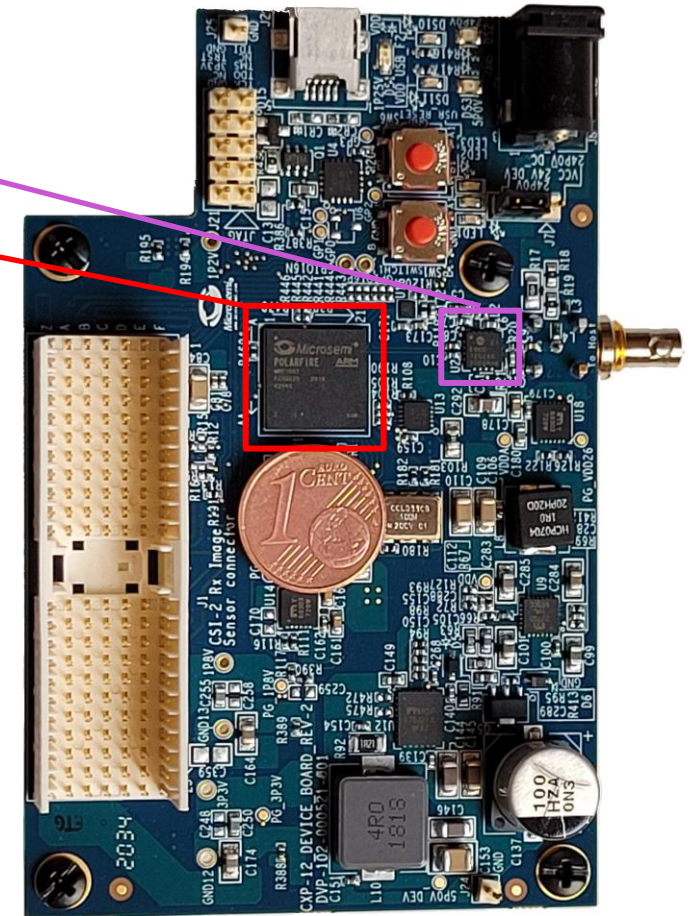
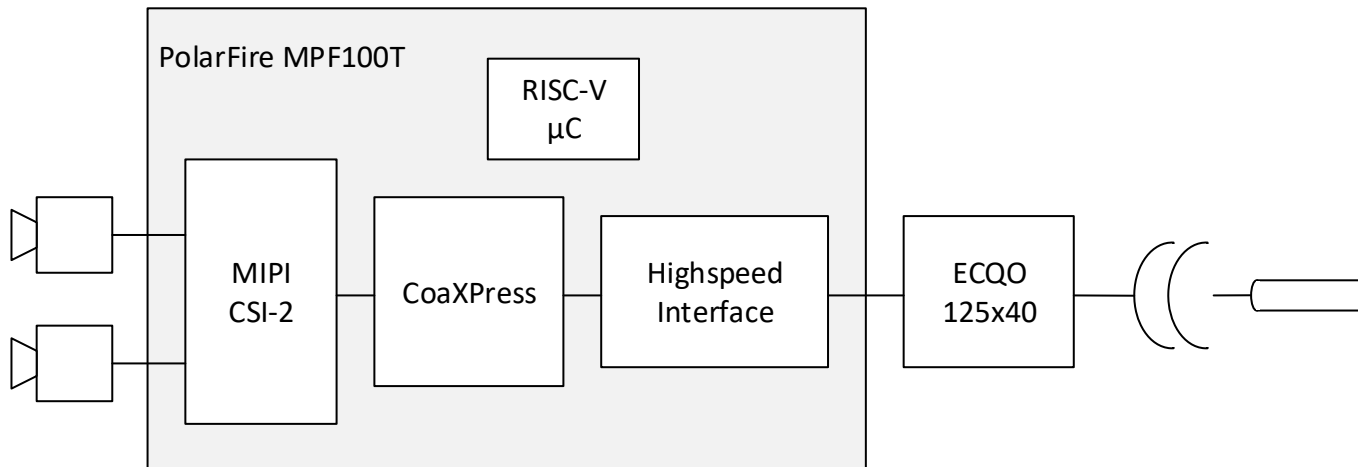
Requirement	Microchip benefit
Small housing	Optimized layout
MIPI CSI-2 4kx60 sensors	Native CSI-2 support
Simple thermal system	Low static, optimized transceivers
Connectivity	Total System Solution



Connected Vision – CoaXPress®

VIDEO-DC-CXP

- EQCO125X40 Transmitter (4x4 mm²)
- PolarFire® MPF100T-FCSG325 (11x11 mm²)
- MIPI CSI-2 to CoaXPress at 12.5 Gbps



Thermal Camera

Key Considerations

Requirement	Microchip Benefit
Handheld, battery-driven	Small power-consumption
Small housing	11x11mm ² no configuration-memory
No interference with sensor	Very small self-heating
Interfacing to thermal sensor	Native MIPI support



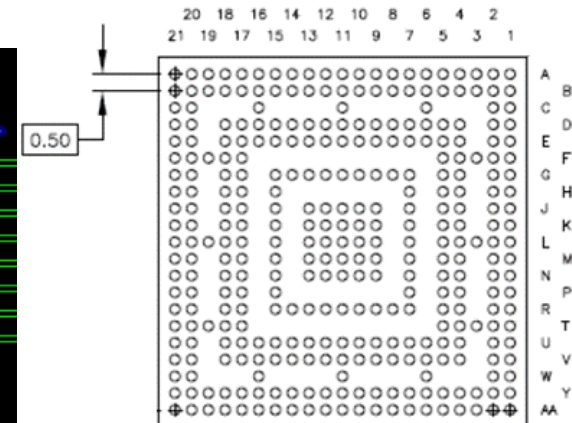
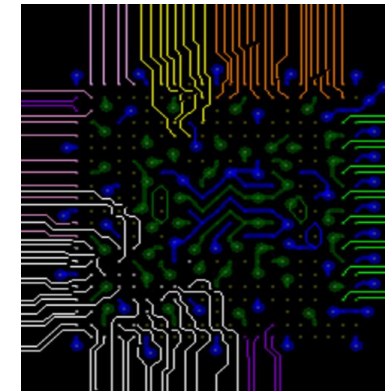
Measurement Equipment

High-Temperature Environment

- Position measurement on motor-shafts
- Control of multiple high-power Silicon Carbide or IGBT power modules



Requirement	Microchip benefit
Mounting in hot environment (95°C)	Small static power
Space constrained	Small packages
Low-cost PCB	Simple PCB-routing
High reliability	SEU immunity

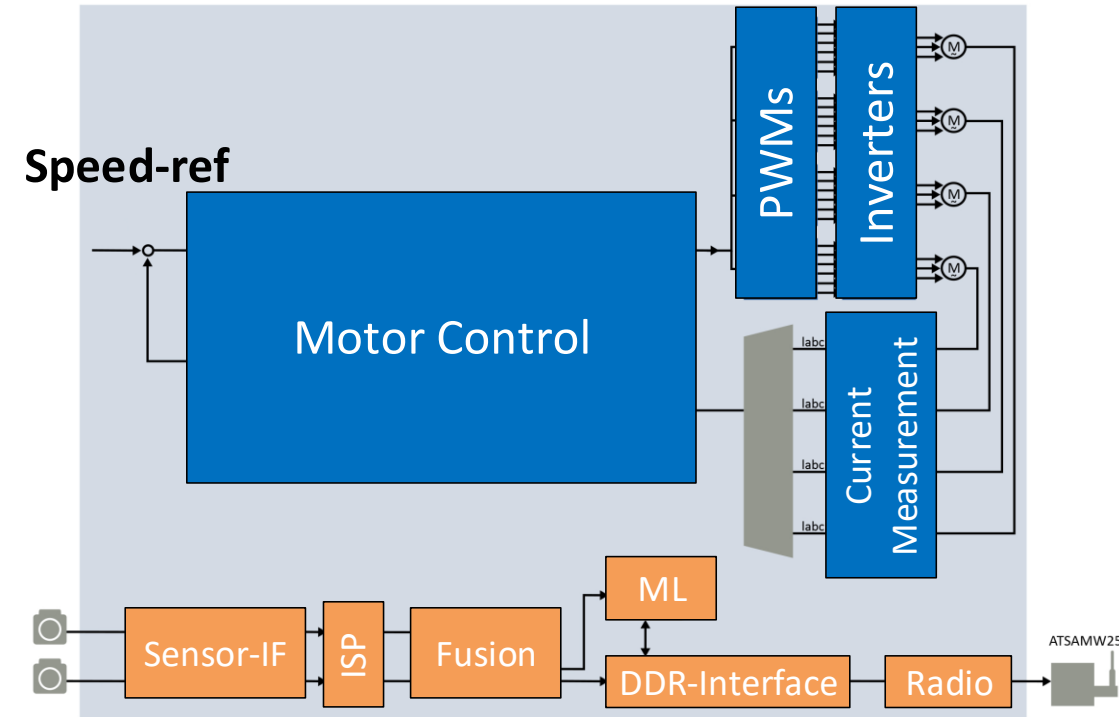


Professional Drones

Flying Connected Sensors



Requirement	Microchip benefit
Long flying time	Small power-consumption
Silent flying	- FOC motor-control IP
Accurate control	- Deterministic fast loop-timing
Multiple sensors	Flexibility of FPGA, native MIPI CSI-2 support
Connectivity	Microchip portfolio



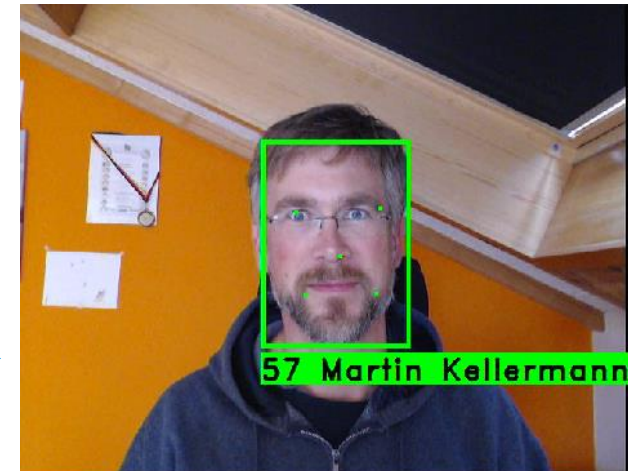
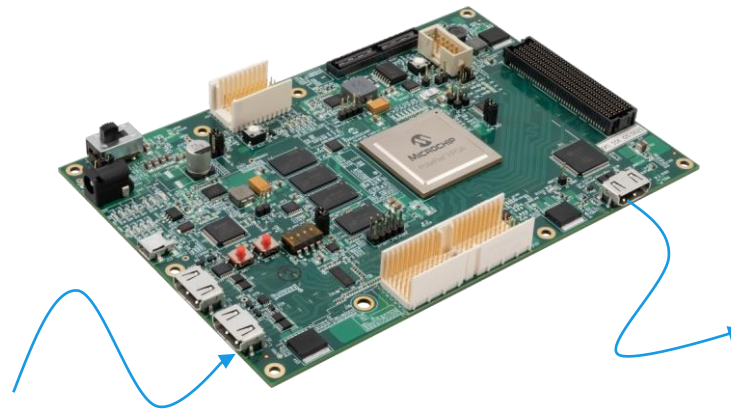
Real world example

PolarFire Video Kit and Machine Learning

Design Example

Person Recognition on MPF300-VIDEO-KIT

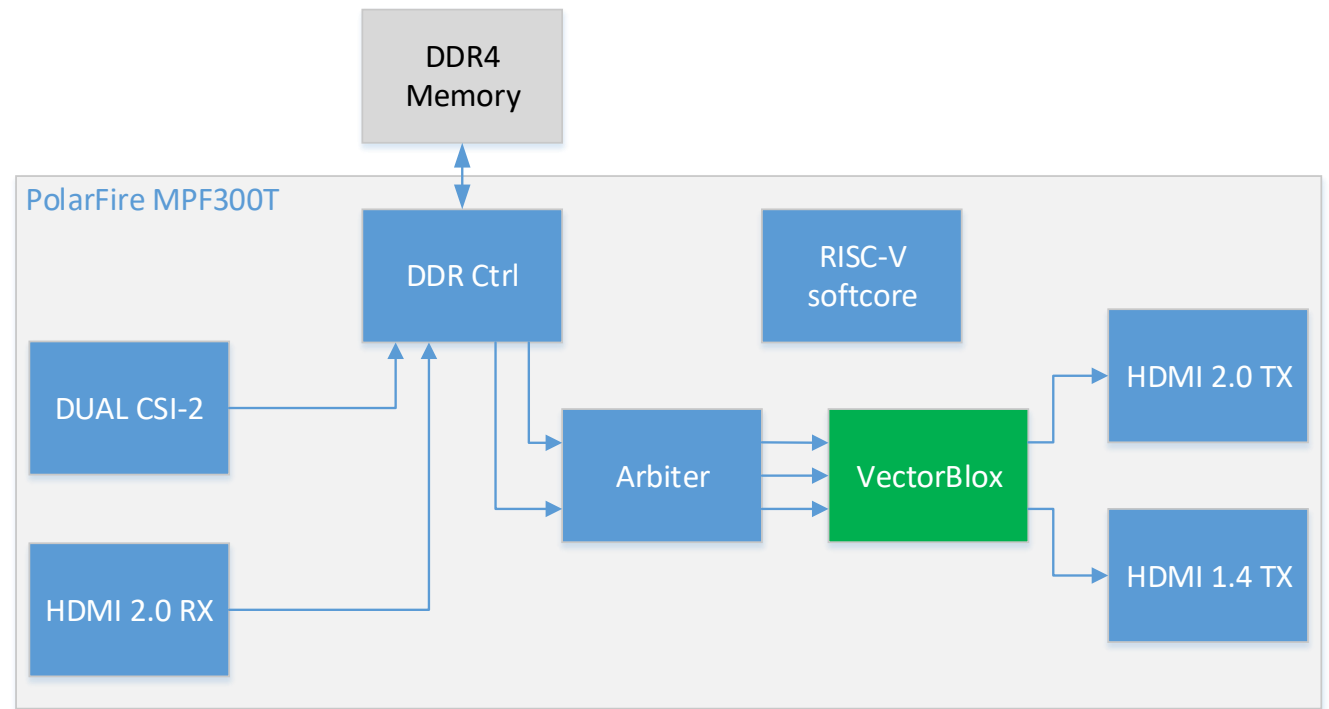
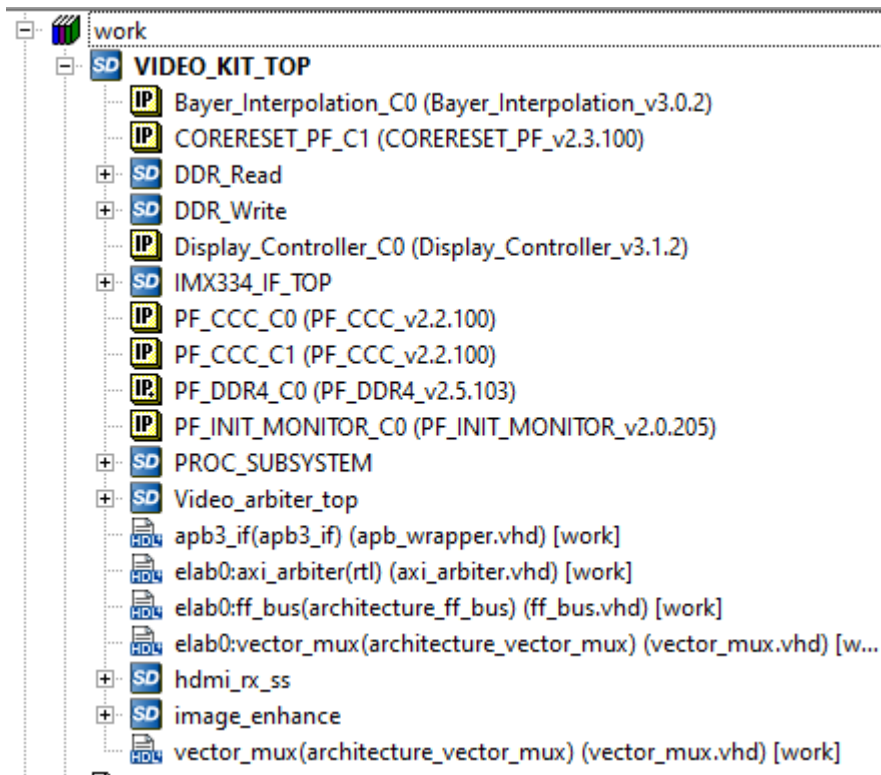
- **Design-Resources, Face Recognition:**
 - Design: https://bit.ly/MCHP_VBX_13
 - SDK: <https://github.com/Microchip-Vectorblox>
- **HDMI in/out**



Block Diagram Face Detection

MPF300-VIDEO-KIT

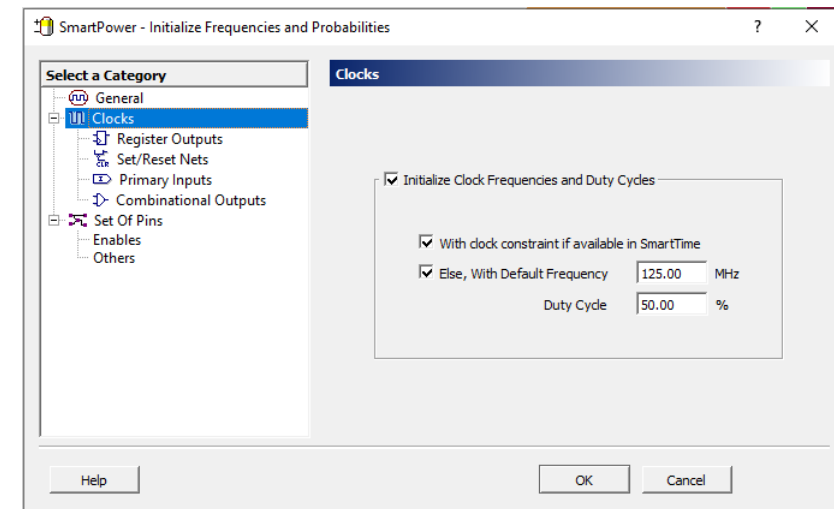
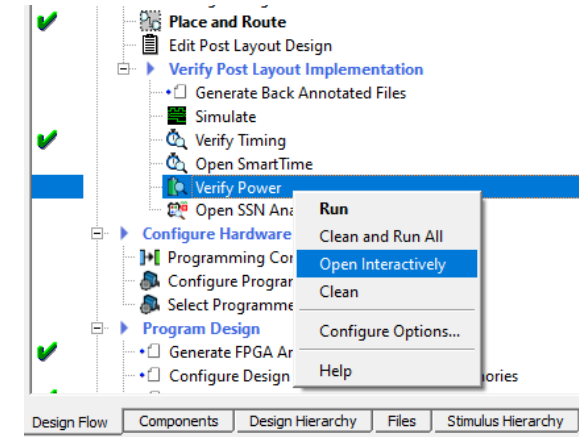
- Libero SoC example design based on DG0849



Power Analysis of Design

SmartPower on Implemented Design

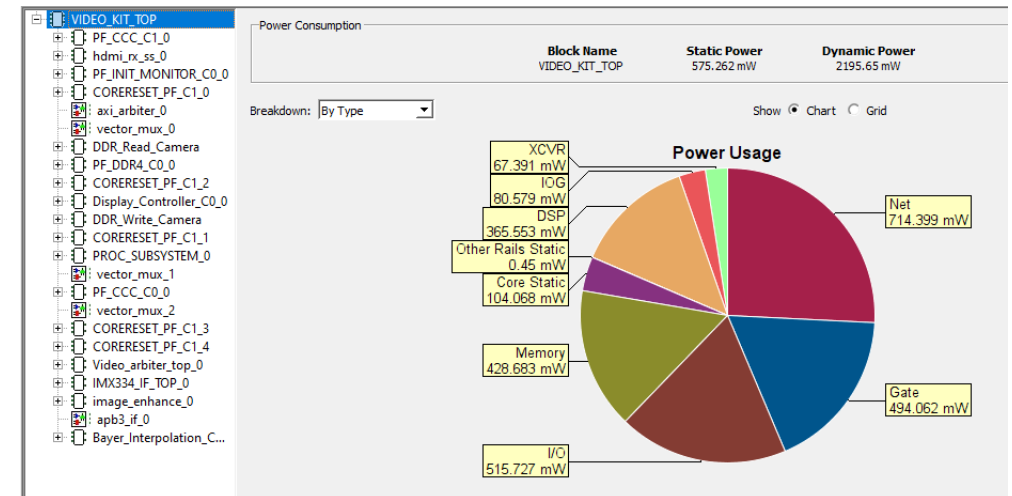
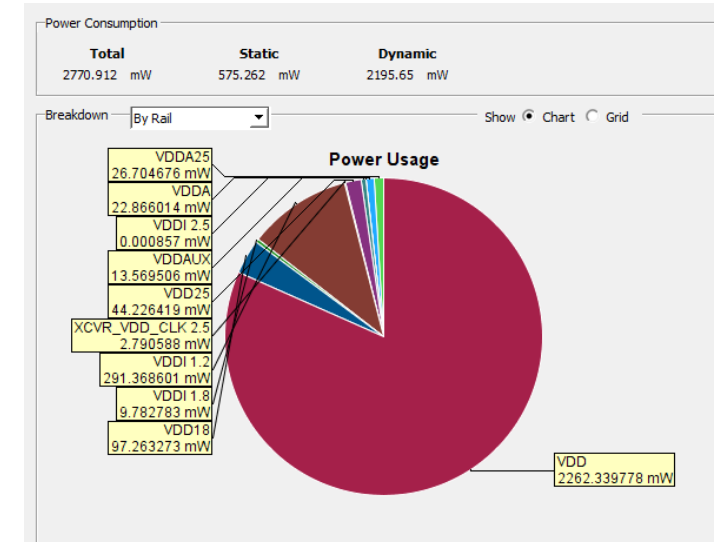
- **SmartPower**
 - Run on implemented design
 - Allows accurate power-analysis on full design and design-blocks
- **Toggle-Rates influencing power**
 - Vector-less propagation
 - Based on netlist simulation
 - Manually



Power Analysis

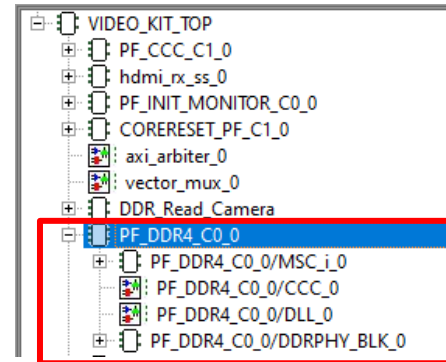
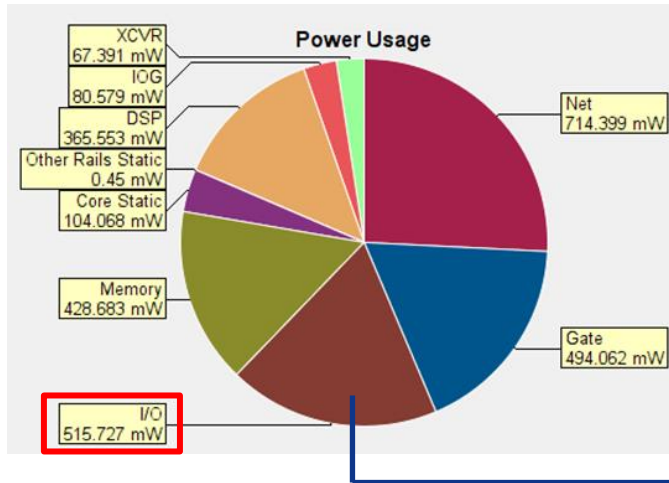
SmartPower for Detailed Block Analysis

- **Summary, by rail**
 - Dimensioning of power supplies
- **Hierarchical Analysis**
 - Where is power consumed
 - What does consume the power

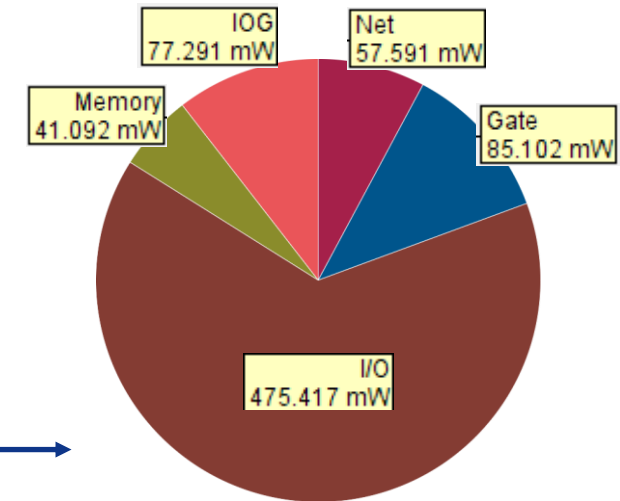


Power Analysis

Diving Into Design, IOs



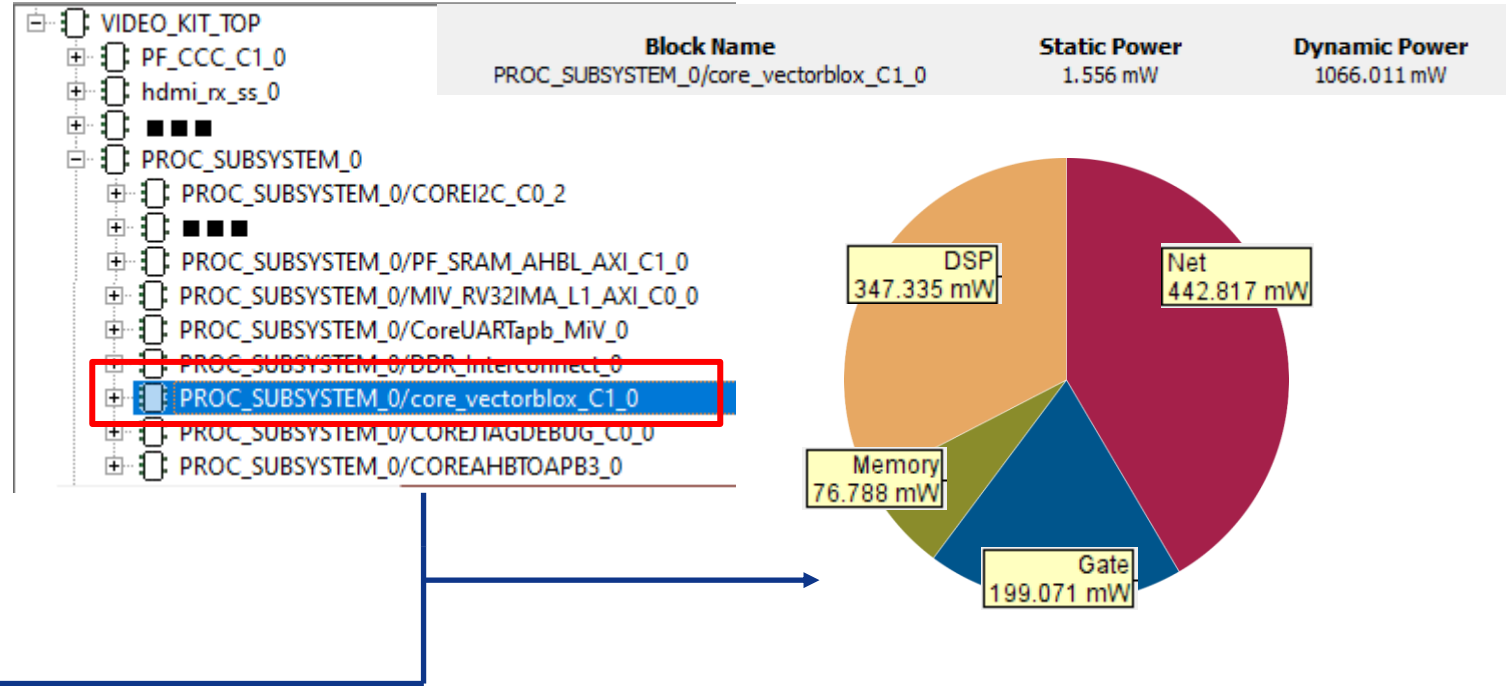
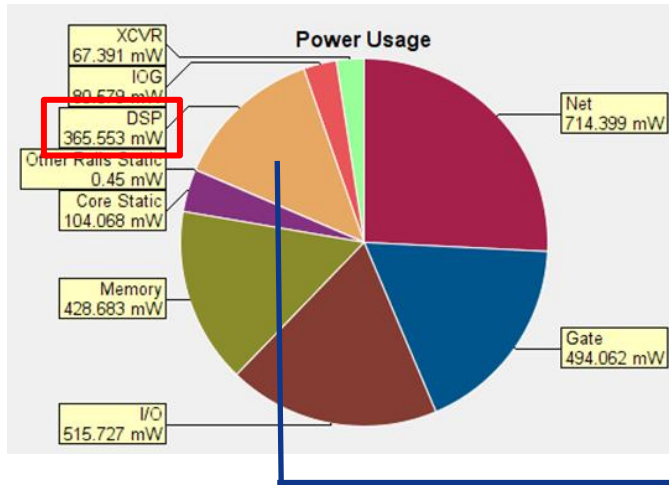
Block Name	Static Power	Dynamic Power
PF_DDR4_C0_0	444.121 mW	292.776 mW



- Breakdown based on design-hierarchy
- Allows analysis on potential power-savings
- DDR-memory is costly on power

Power Analysis

Diving Into Design, DSPs

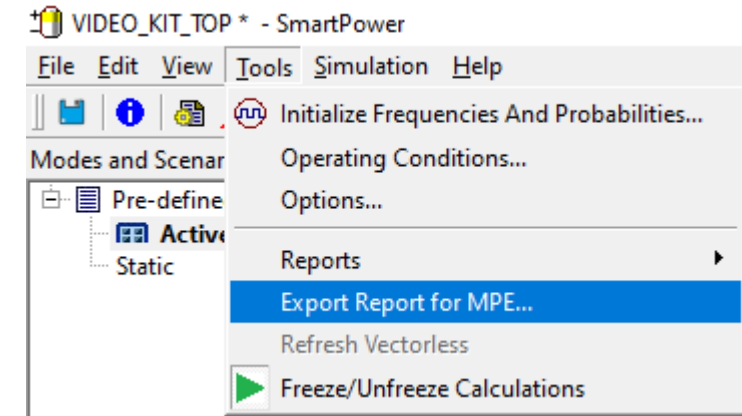


- VectorBlox Machine Learning IP highest contributor to power consumption
- 1066 mW for Machine Learning IP => Low Power Machine Learning

Environmental What-If

Excel-based Power Estimator

- Export from SmartPower to Microchip Power Estimator (MPE)



- Import into MPE

bit.ly/MCHP_MPE



- Allows analysis for device and environment changes



Thermal Inputs	
Calculation mode	Estimated Tj
Ambient Temperature Ta (°C)	25.00
Theta JA	Estimated Theta JA
Effective Θ_{JA} (°C/W)	8.00
Heat Sink	None
Air Flow	Still Air
Custom Θ_{SA} (°C/W)	
Board Thermal Model	JEDEC (2s2p)

Power Summary	
Summary	
Total Power (W)	2.593
→ Device Static (W)	0.160
→ Core Dynamic (W)	1.810
→ I/O (W)	0.563
→ Transceiver (W)	0.059
Junction Temperature Tj (°C)	45.75
Effective Theta JA (°C/W)	8.00
Thermal Margin	Maximum Ta (°C) 76.19
	Maximum Power (W) 9.37

Design-Based What-If

Low-Effort Power Estimation

- Checking on return before redesign

- Toggle-rates
- Clock-rates
- IO-settings

$T_j = 45.8^{\circ}\text{C}$

Name	Clock Frequency (MHz)	Number of DFF	Number of 4LUT	Design Complexity	Toggle Rate	Power (W)
PROC_SUBSYSTEM_0/COREJTAGG	30.00		209	2.1	13.4%	0.000
PROC_SUBSYSTEM_0/COREJTAGG	30.00	337		1.5	12.4%	0.000
PF_CCC_C0_0/PF_CCC_C0_0/pll_ins	137.50	10833		1.9	12.4%	0.021
PF_CCC_C0_0/PF_CCC_C0_0/pll_ins	275.00		27000	1.5	12.6%	0.069
PF_CCC_C0_0/PF_CCC_C0_0/pll_ins	275.00	42196		1.5	12.4%	0.133
IMX334_IF_TOP_0/PF_CCC_C2_0/PFJ	120.00		2747	1.4	13.3%	0.003
IMX334_IF_TOP_0/PF_CCC_C2_0/PFJ	120.00	1466		2.2	12.4%	0.003

$T_j = 46.9^{\circ}\text{C}$

Name	Clock Frequency (MHz)	Number of DFF	Number of 4LUT	Design Complexity	Toggle Rate	Power (W)
PROC_SUBSYSTEM_0/COREJTAGG	30.00		209	2.1	13.4%	0.000
PROC_SUBSYSTEM_0/COREJTAGG	30.00	337		1.5	12.4%	0.000
PF_CCC_C0_0/PF_CCC_C0_0/pll_ins	137.50	10833		1.9	12.4%	0.021
PF_CCC_C0_0/PF_CCC_C0_0/pll_ins	275.00		27000	1.5	12.6%	0.069
PF_CCC_C0_0/PF_CCC_C0_0/pll_ins	275.00	42196		1.5	25.0%	0.269
IMX334_IF_TOP_0/PF_CCC_C2_0/PFJ	120.00		2747	1.4	13.3%	0.003
IMX334_IF_TOP_0/PF_CCC_C2_0/PFJ	120.00	1466		2.2	12.4%	0.003

Comparing to other architectures

Power Estimation Tools

- How do other architectures behave?
- Can I estimate without doing a large design-run?

Settings	
General	
Family	PolarFire
Device	MPF300T
Package	FCG1152
Range	Extended
Core Voltage	1.0 V
Process	Typical
Speed Grade	-1
Data State	Production

Settings	
Device	
Family	
Device	XC7K325T
Package	FBG900
Speed Grade	-2L
Temp Grade	Extended
Process	Typical
Voltage ID Used	
Characterization	Production

Settings	
Device	
Family	
Device	XCKU5P
Package	FFVA676
Speed Grade	-1
Temp Grade	Industrial
Process	Typical
Voltage ID Used	
Characterization	Production (± 15% accuracy)

- ➔ Power estimation tools are your friends
- ➔ Copy/Paste + adaption for comparison = medium effort

Power Estimation Tools

Comparing results

- Goal: have common information for direct comparison

bit.ly/mchp_convert



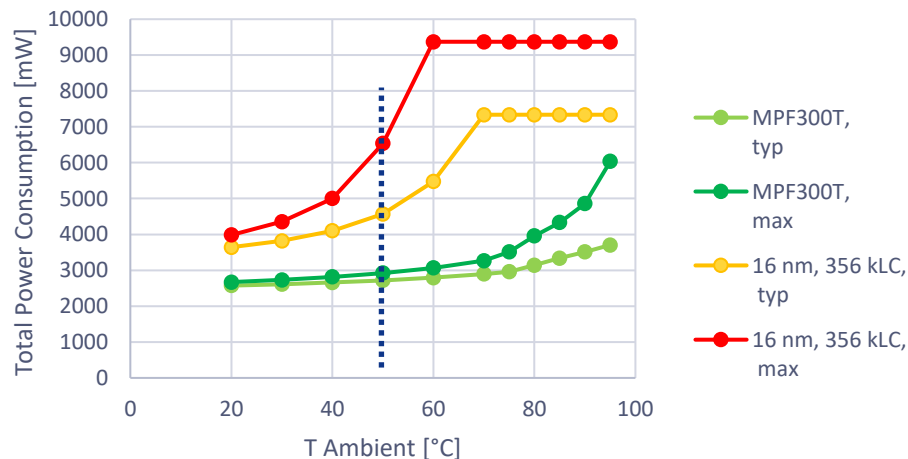
Microchip Power Comparison Tool	
Name of Microchip Power Estimator	MPE_Person_Detection.xlsm
Name of Xilinx Power Estimator	XPE_7_Person_Detection.xlsm
Source Architecture	7 Series
Average Depth of Shift Registers	5
Theta Junction Ambient [°C/W]	8
<input checked="" type="checkbox"/> Set Theta JA in Estimators	TRUE
If tickbox is set then the Tja-value from cell B12 is used in both estimators.	

1) Transfer XPE 2 MPE

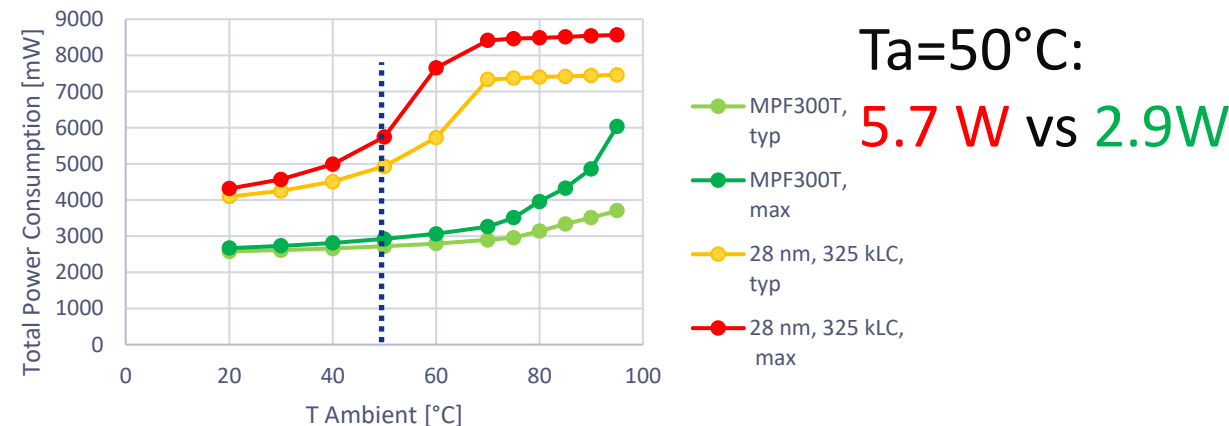
2) Create Power Comparison

- Result: Temperature sweeps for bigger picture

Power Consumption vs. Ambient Temperature



Power Consumption vs. Ambient Temperature



Power Estimation and Temperature

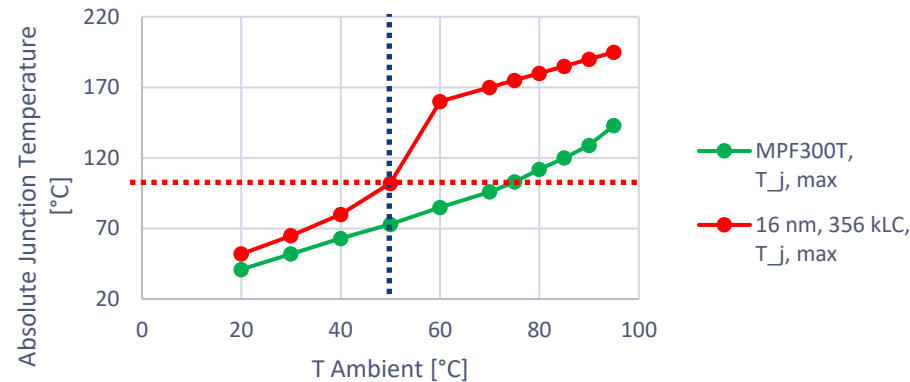
System Environmental Condition

$T_a = 50^\circ\text{C}$:

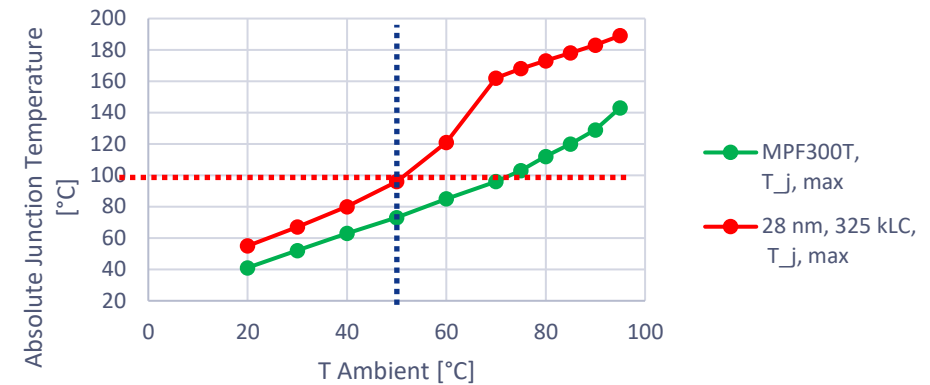
$>100^\circ\text{C}$ vs 70°C

Temperature
sweeps allow
behavior-
comparisons

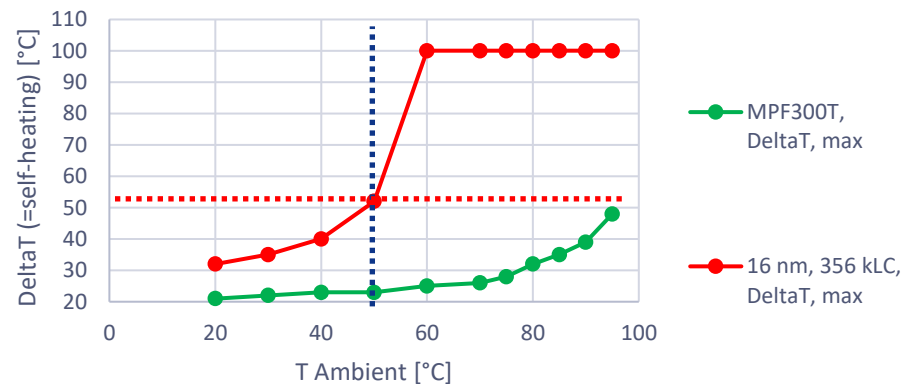
Absolute Temperature vs. Ambient Temperature



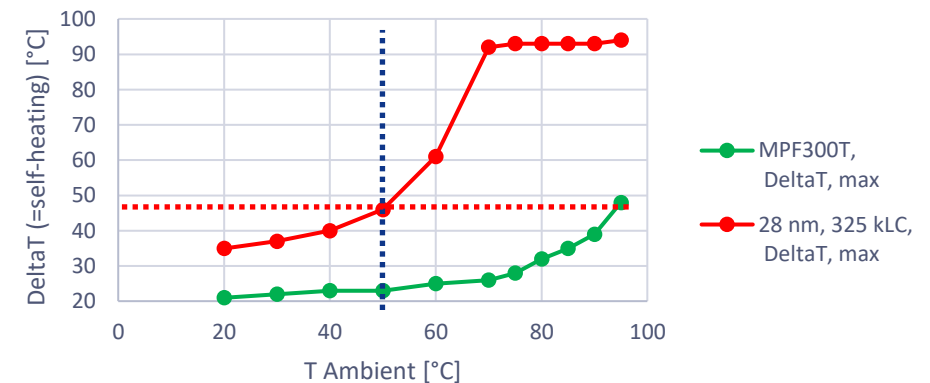
Absolute Temperature vs. Ambient Temperature



DeltaT vs. Ambient Temperature

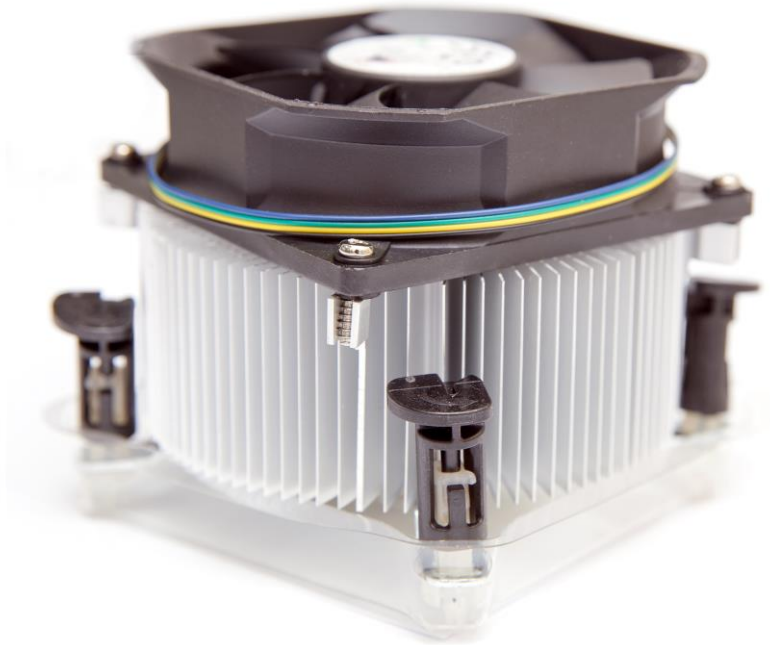


DeltaT vs. Ambient Temperature



System Implication

- Resulting Junction Temperature $>100^{\circ}\text{C}$ vs. 70°C



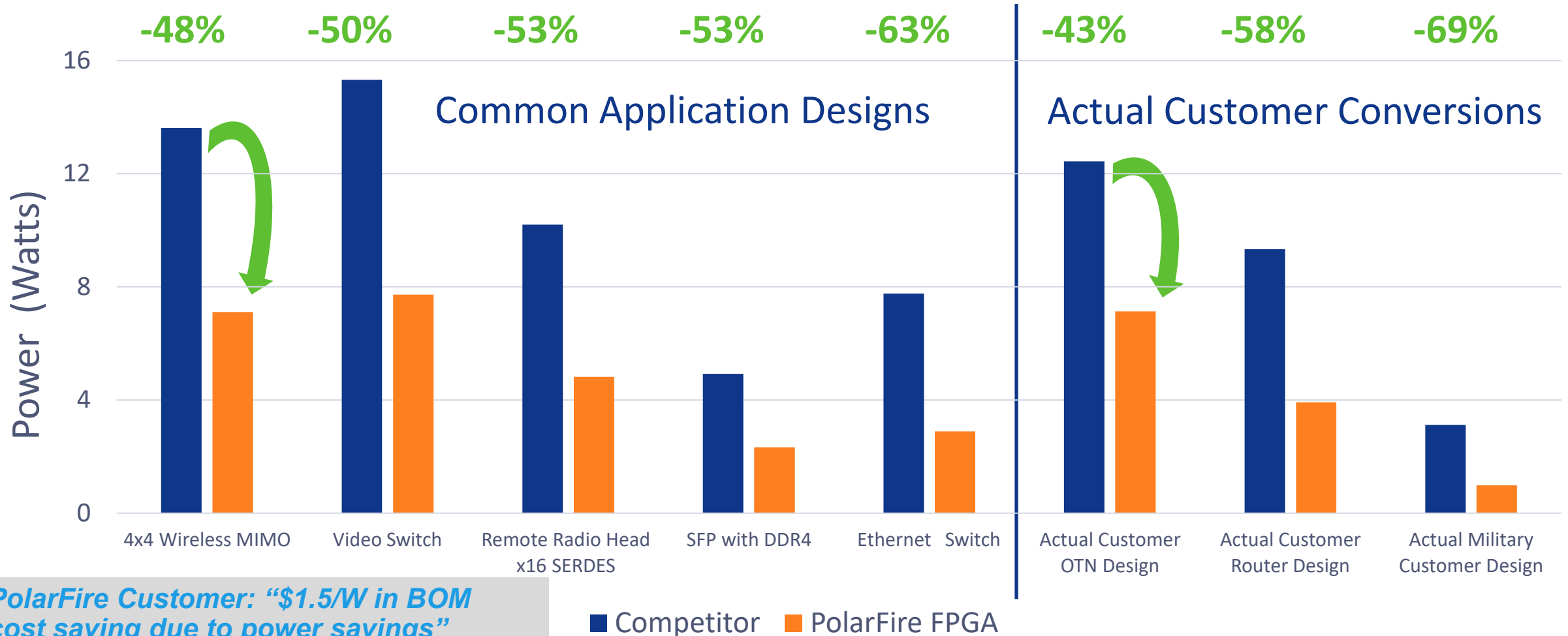
SRAM FPGA add-on kit



PolarFire video kit

PolarFire® Power Savings by Design

Lowest Power – Saving 43% to 69% Versus Competition



All designs using official layout and power estimation tools with common effort levels

All designs using PolarFire standard speed devices versus low-power-binned devices; similar performance devices)

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Summary

Microchip Advantage on Power/Watt

- Microchip FPGAs provide significant power-advantage over competition
- Lower power = less trouble
- Significantly lower power = system benefit
- You can see on your own existing design



Q&A

Thank You

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