AN4723

PolarFire SoC FPGA Video Kit Picture-In-Picture Appication Note

Introduction (Ask a Question)

This application note describes the method to run the imaging and video demo using the PolarFire® SoC video kit, a dual camera sensor module, and an HDMI monitor. This solution is developed on Microchip's PolarFire SoC video kit, which features an MPFS250TS PolarFire SoC device.

The demo demonstrates the following features:

- MIPI CSI-2 RX to read the Full HD dual-camera input
- Color Filter Array (CFA) to Red, Green, Blue (RGB) conversion
- Display Controller
- Picture-in-Picture (PIP)
- Full HD video output via HDMI 2.0 TX port
- Edge detection
- Histogram
- Image enhancements such as contrast, brightness, color balance, and gamma correction

The demo includes a user-friendly Video Control Graphical User Interface (GUI) to control the image and video settings.

PolarFire SoC video kit enables prototyping of Video and Imaging solutions. It supports the following key features among others:

- MPFS250TS PolarFire SoC device
- MIPI CSI-2 interface
- FPGA Mezzanine Card (FMC) connector
- SD and eMMC card, LPDDR4, and DDR4 memories
- HDMI, Ethernet, PCIe, and other interfaces

For more information about the PolarFire SoC video kit, see MPFS250-VIDEO-KIT.

© 2023 Microchip Technology Inc. and its subsidiaries

Table of Contents

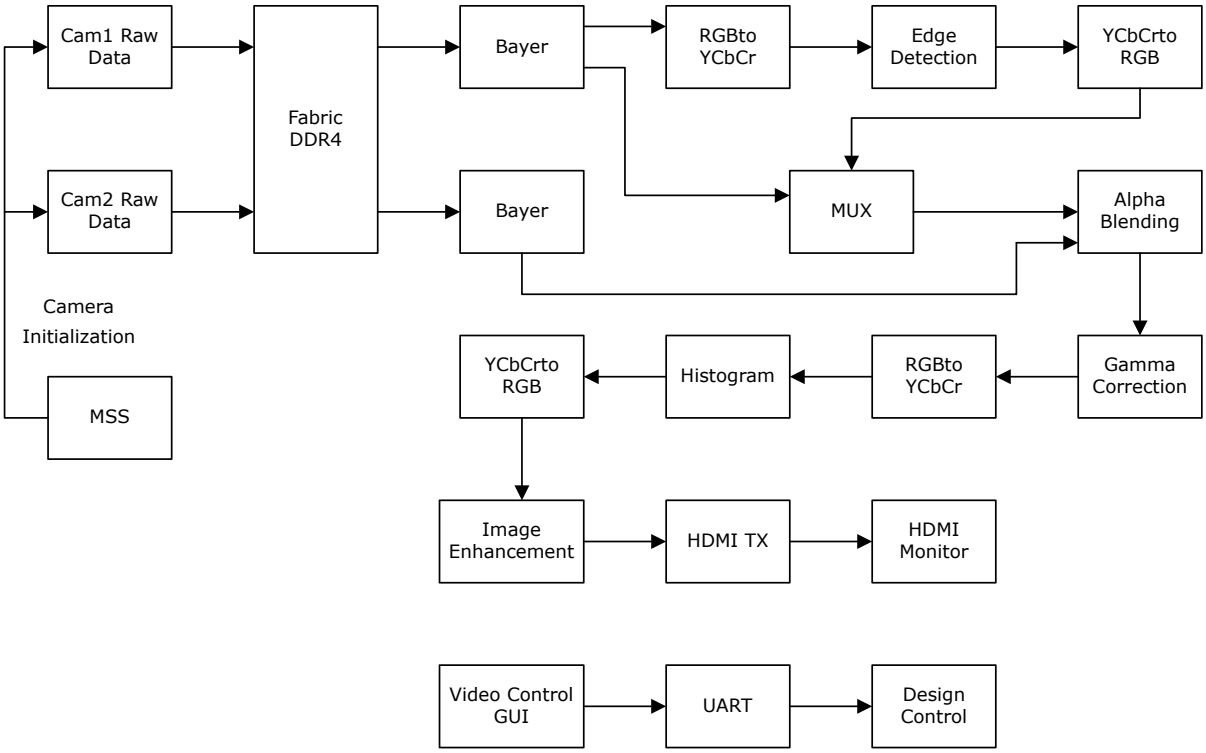
© 2023 Microchip Technology Inc. and its subsidiaries

1. Design Overview (Ask a Question)

The following figure shows the top-level block diagram of the reference design. The raw data is captured from a dual camera sensor module and is written into the fabric DDR4 memory. The raw data undergoes through image processing pipeline IPs such as Bayer, RGBtoYCbCr, YCbCrtoRGB, Edge Detection, Image Enhancement, and so on. The processed data is then blended from both the camera modules with an alpha blending IP before displaying it onto a HDMI compliant device. Microprocessor Sub-System (MSS) runs the firmware code, which enables in configuring both the camera sensor modules through I^2C channels.

The live video can be updated for various features such as brightness, contrast, and so on with the help of video control GUI. This GUI communicates with the design on the board through UART.

Figure 1-1. Top-Level Block Diagram



1.1 IP Blocks (Ask a Question)

The following table lists the IP blocks used in the design and their functionality.

Table 1-1. IP Blocks

IP Block	Description
PF_OSC_C0	This PolarFire® RC Oscillator generates a 2 MHz clock.
PF_CCC_C0	This PolarFire Clock Conditioning Circuit (CCC) block generates required clocks in the design.
PF_CLK_DIV_C0	This clock divider block is used in divide by 2 configuration.
PF_DDR4	This fabric DDR4 controller block writes or reads video to on-board DDR4 (x64).
Edge_Detection_C0	This IP block detects edge of the objects seen in camera.
YCbCrtoRGB_C0	This color space conversion IP block converts YUV444 24-bit data format to RGB 24-bit data format.
Alpha_Blending_C0	This IP block emphasizes second camera video (PIP) in the main first camera video depending on the input configuration value of alpha.
Histogram_C0	This IP block plots the histogram graph of the incoming data frame.
PF_IOD_Generic_RX	This IP block operates with 1200 Mbps data rate.
CORERESET_PF	This IP block synchronizes the reset to the respective clock domain.
VK_MSS	This is the hard MSS block on the PolarFire SoC FPGA. It helps in configuring both the camera sensor modules present on the daughter board of the video kit, which is used in PIP application. It can be configured using MSS configurator. For more information about the MSS configuration, see 1.2. MSS Configuration.
RGBtoYCbCr_C0	This color space conversion IP block converts RGB 24-bit data format to YUV444 24-bit data format.
Video_arbiter_top_0	This module arbitrates the fabric DDR4 memory access between DDR_Write packaging module and DDR_Read unpackaging module. The arbitration is based on the round robin scheduling algorithm. The packaging modules forward the raw 32-bit data to the arbiter. The unpackaging modules request the raw 32-bit data for processing. The arbiter interfaces with the DDR4 controller and performs read and write operations to DDR4.
HDMI_TX_C0_0	This IP block receives the 24-bit RGB HD data and encodes it to 30-bit Transition-Minimized Differential Signaling (TMDS) data.
intensity_average	This module calculates average value of the pixel data in the current frame from the camera.
alpha_enable	This module latches value of alpha based on the input enable signal.
apb3_slv_if	This module configures various parameters of the live video and design functionality using Video Control GUI.
Bayer_Interpolation_C0_0/ Bayer_Interpolation_C1_0	This IP block converts the 8-bit raw data to 24-bit RGB data.
Gamma_Correction	This IP block converts the pixel intensity to match with the perspective of human eye by using a logarithmic curve.
Image_Enhancement	This IP block adjusts the brightness, contrast, and color balance through user controls.

.....continued	
IP Block	**Description**
Display_Controller	This IP block generates sync signals for full HD resolution (1920x1080).
PF_XCVR_ERM_C2_0	This IP block receives the 30-bit TMDS data from HDMI Tx IP and displays on the HDMI compliant display device.
pip_mode_0	This RTL captures shift-related inputs for the scaled PIP camera data.
UART_interface_0	This SmartDesign module receives data from the Video Control GUI, which enables in controlling and modifying the design-related parameters in the live running demo.
DDR_Write_1/DDR_Write_0	This SmartDesign module packages the 32-bit raw data into a Bayer-complaint 512-bit data line and writes it to the DDR4 memory via fabric DDR4 controller using the AXI4 interface.
DDR_Read_1	This SmartDesign module reads the Bayer compliant 512-bit data line from the arbiter and unpackages the 512-bit data (64 bytes) to 8-bit raw data (one pixel). This 8-bit data is forwarded to the Bayer Interpolation IP.
IMX334_IF_TOP	This SmartDesign module receives the dual live camera feed from both the camera sensors present on the daughter board and converts it into raw 32-bit parallel data. Each 32-bit parallel data encapsulates four pixels data (each byte representing one pixel).
PF_XCVR_REF_CLK	This IP block takes the differential clock of 148.5 MHz from on-board clock source and converts it to single-ended clock source with same frequency.
PF_TX_PLL	This IP block uses a reference clock of 148.5 MHz to get output bit clock of 5940 Mbps.
INIT_MONITOR	This IP block triggers reset to the design.
CoreAPB3_C0_0	This IP block connects the APB slave module with MSS.

1.2 MSS Configuration (Ask a Question)

The following table lists the configuration of MSS clock, peripherals, and memory.

Table 1-2. MSS Configuration

MSS Block	Description
MSS Clocks	MSS PLL reference clock source: 125 MHz MSS CPU clock frequency: 600 MHz
Peripherals	I^2C: Used for initializing the camera
Fabric Interface Controller (FIC)	FIC3_APB_Master: Accessing camera control registers through APB interface
Low Power DDR4 memory (LPDDR4)	Low Power DDR4 memory is unused in this Picture-in-Picture design
Memory Partitioning	Since LPDDR4 is unused, memory partitioning is not used in the current design

1.3 I/O Ports (Ask a Question)

The following table lists the key I/O ports in the design.

Table 1-3. I/O Ports

Port Name	Direction	Description
CAM1_RST/CAM2_RST	Output	Resets the camera sensor module.
CAM1_RX_CLK_P CAM1_RX_CLK_N	Input	Input pads to receive the reference clock for the camera sensor module.
CAM2_RX_CLK_P CAM2_RX_CLK_N	Input	Input pads to receive the reference clock for the camera sensor module.
CAM1_RXD[0] CAM1_RXD_N[0] CAM1_RXD[1] CAM1_RXD_N[1] CAM1_RXD[2] CAM1_RXD_N[2] CAM1_RXD[3] CAM1_RXD_N[3]	Input	Input pads to receive the live video from the camera sensor module. These pads are assigned to the Bank 7 I/Os.
CAM2_RXD[0] CAM2_RXD_N[0] CAM2_RXD[1] CAM2_RXD_N[1] CAM2_RXD[2] CAM2_RXD_N[2] CAM2_RXD[3] CAM2_RXD_N[3]	Input	Input pads to receive the live video from the camera sensor module. These pads are assigned to the Bank 7 I/Os.
MSS Peripheral Ports		
REFCLK REFCLK_N	Input	Input ports for receiving MSS reference clock from the on-board 125 MHz oscillator.
I2C 0/1	Input/Output	I^2C interface signals for the dual sensor camera module.
FIC3_APB_INITIATOR	Output	Writes to apb_slave_if module.
GPIO_2_(2-3)	Output	GPIO signals are connected to LEDs.
GPIO_2_4	Output	Resets the IMX module after camera training is done.
GPIO_2_7	Output	Resets CAM2 sensor.
GPIO_2_8	Output	Resets CAM1 sensor.
GPIO_2_9	Output	Enables the clock to the daughter card camera module.
Transceiver Ports		
REF_CLK_PAD_N REF_CLK_PAD_P	Input	Input ports for receiving the transceiver reference clock. These ports are assigned to AF29 and AF30 pins, which are connected to the on-board 148.5 MHz oscillator.

© 2023 Microchip Technology Inc.
and its subsidiaries

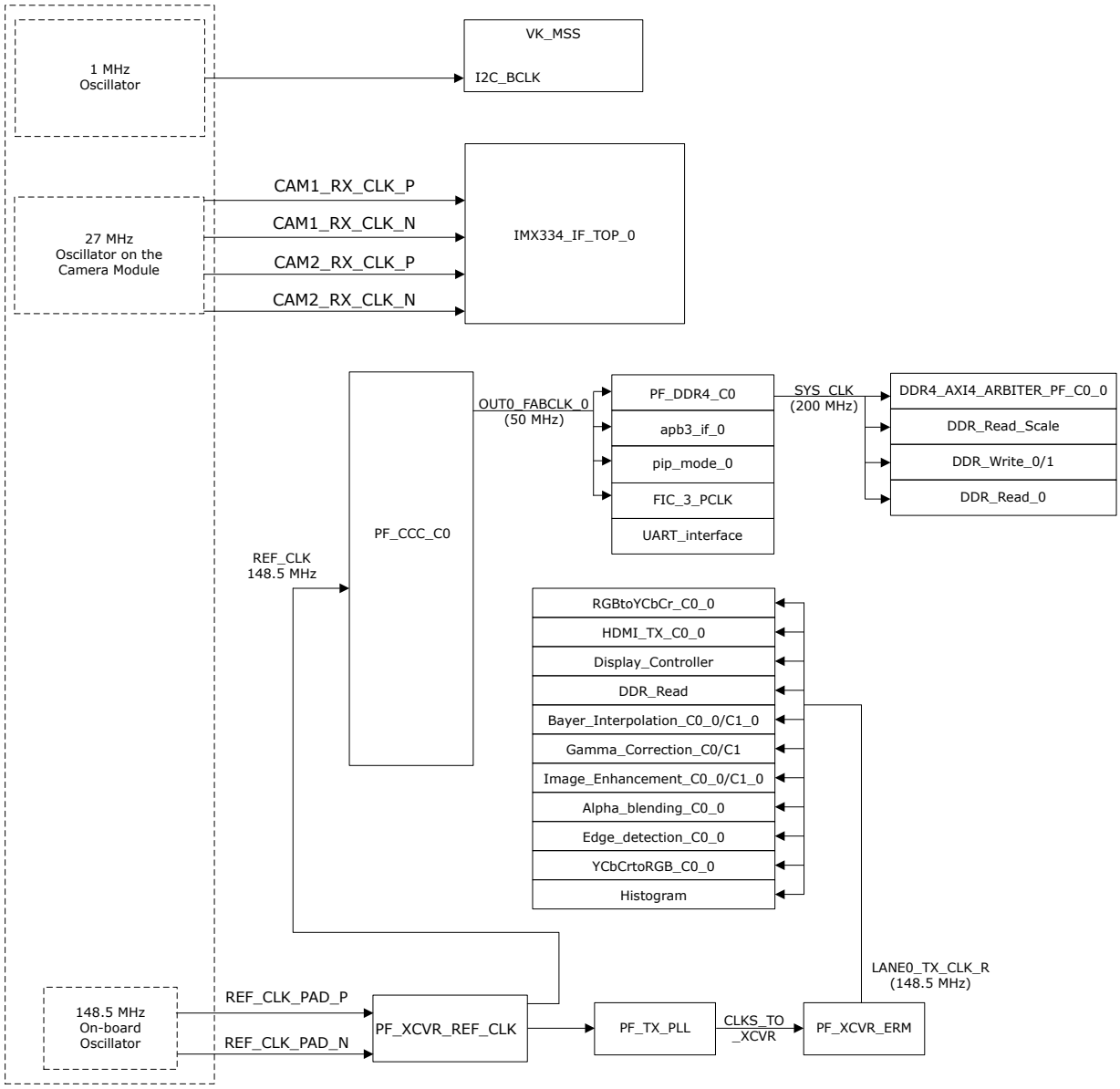
.....continued		
Port Name	**Direction**	**Description**
LANE0_TXD_N LANE0_TXD_P LANE1_TXD_N LANE1_TXD_P LANE2_TXD_N LANE2_TXD_P LANE3_TXD_N LANE3_TXD_P	Output	Transceiver TX lanes connected to HDMI TX interface.

© 2023 Microchip Technology Inc.
and its subsidiaries

1.4 Clocking Structure (Ask a Question)

The following figure shows the clocking structure of the design. PF_CCC_C0 generates the 50 MHz fabric clocks from the REF_CLK generated by PF_XCVR_REF_CLK. This clock drives the APB3 bus interface and provides the reference clock for the PLL inside the PF_DDR4 Controller. The on-board 148.5 MHz on-board oscillator provides a reference clock to generate clocks used in the design.

Figure 1-2. Clocking Structure

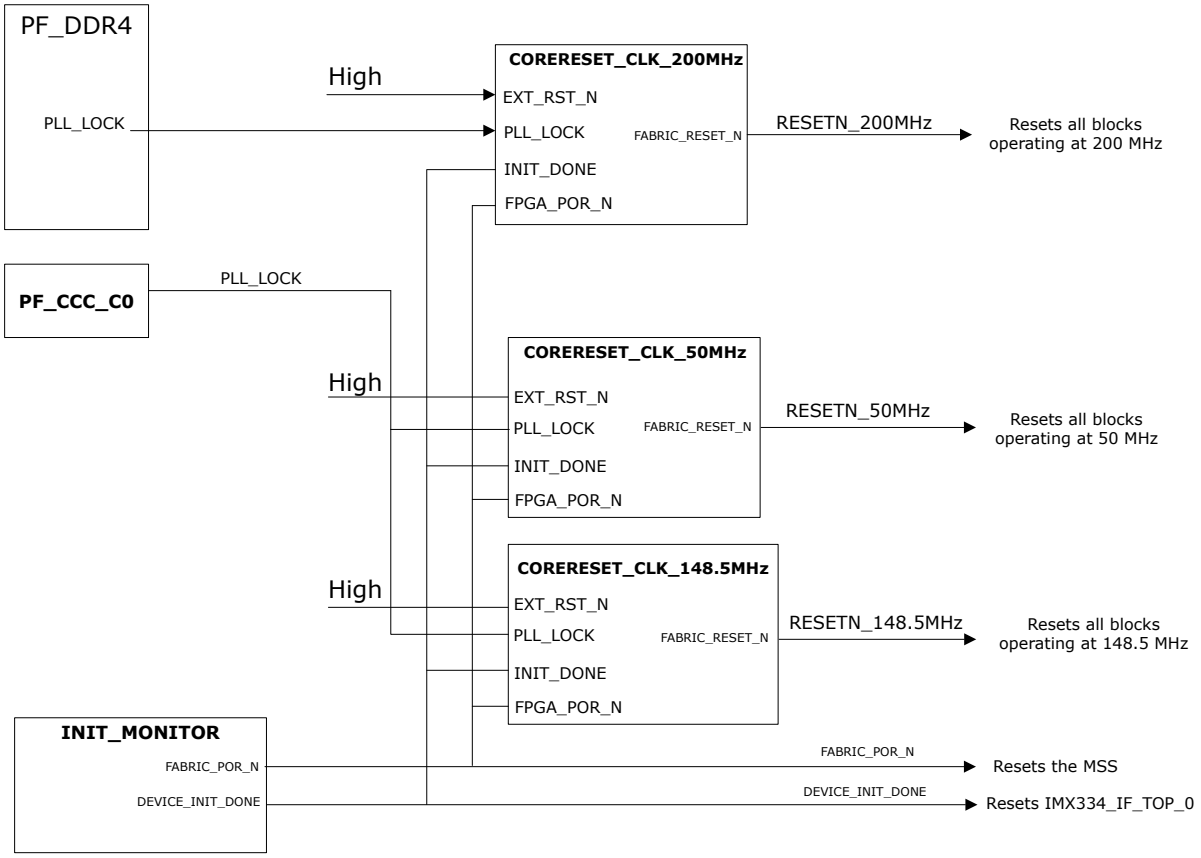


1.5 Reset Structure (Ask a Question)

The following figure shows the reset structure of the design. The INIT_MONITOR IP asserts the following signals:

- FABRIC_POR_N: Asserted after the initialization of the fabric. FABRIC_POR_N is used to reset MSS.
- DEVICE_INIT_DONE: Asserted after the initialization of the PolarFire SoC device.

Figure 1-3. Reset Structure



1.6 Resource Utilization (Ask a Question)

The following figure shows the resource utilization of the design.

Figure 1-4. Resource Utilization

Module Name	Fabric 4LUT	Fabric DFF	Interface 4LUT	Interface DFF	Single-Ended I/O	Differential I/O Pairs	uSRAM 1K	LSRAM 18K	Math (18x18)	Chip Globals	Row Global	PLL	DLL	Transceiver Lanes
Top	52233	45949	7704	7704	120	20	66	165	27	17	4	3	1	4
Primitives	1	18	0	0	11	0	0	0	0	0	0	0	0	0
CLOCKS_AND_RESETS_0	2	34	0	0	0	0	0	0	0	5	0	1	0	0
DDR_AXI4_ARBITER_P...	2429	2805	480	480	0	0	1	13	0	0	0	0	0	0
DDR_Read_0	728	779	468	468	0	0	0	13	0	0	0	0	0	0
DDR_Read_1	559	431	180	180	0	0	0	5	0	0	0	0	0	0
DDR_Write_0	644	691	468	468	0	0	0	13	0	0	0	0	0	0
DDR_Write_1	644	691	468	468	0	0	0	13	0	0	0	0	0	0
IMX334_IF_TOP_0	11590	9984	792	792	0	10	0	22	0	7	0	1	0	0
PF_DDR4_C0_0	31813	28362	3264	3264	105	9	65	69	0	4	0	1	1	0
PROC_SUBSYSTEM_0	46	0	0	0	4	1	0	0	0	0	0	0	0	0
UART_interface_0	270	472	0	0	0	0	0	0	0	0	0	0	0	0
COREUART_C0_0	91	80	0	0	0	0	0	0	0	0	0	0	0	0
addr_decoder_0	24	160	0	0	0	0	0	0	0	0	0	0	0	0
ram_read_uart_0	60	70	0	0	0	0	0	0	0	0	0	0	0	0
receive_data_0	21	62	0	0	0	0	0	0	0	0	0	0	0	0
send_data_0	47	83	0	0	0	0	0	0	0	0	0	0	0	0
timer_0	27	17	0	0	0	0	0	0	0	0	0	0	0	0
Video_Processing_0	3503	1682	1584	1584	0	0	0	17	27	1	4	0	0	4
Primitives	1	0	0	0	0	0	0	0	0	0	0	0	0	0
Alpha_Blending_C0_0	56	34	216	216	0	0	0	0	6	0	0	0	0	0
Bayer_Interpolation...	682	304	108	108	0	0	0	3	0	0	0	0	0	0
Bayer_Interpolation...	682	304	108	108	0	0	0	3	0	0	0	0	0	0
CORERESET_PF_C0_0	1	17	0	0	0	0	0	0	0	1	0	0	0	0
CORERESET_PF_C3_0	0	16	0	0	0	0	0	0	0	0	0	0	0	0
Display_Controller_...	148	80	0	0	0	0	0	0	0	0	0	0	0	0
Edge_Detection_C0...	360	144	216	216	0	0	0	6	0	0	0	0	0	0
Gamma_Correction...	366	26	0	0	0	0	0	0	0	0	0	0	0	0
HDMI_TX_C0_0	474	216	108	108	0	0	0	3	0	0	0	0	0	0
Image_Enhanceme...	27	65	108	108	0	0	0	3	0	0	0	0	0	0
MUX_2_to_1_0	24	0	0	0	0	0	0	0	0	0	0	0	0	0
PF_XCVR_ERM_C2_0	0	0	0	0	0	0	0	0	0	0	4	0	0	4
RGB2YCbCr_C0_0	85	51	324	324	0	0	0	0	9	0	0	0	0	0
RGB2YCbCr_C1_0	28	19	108	108	0	0	0	0	3	0	0	0	0	0
YCbCr2RGB_C0_0	134	85	180	180	0	0	0	0	5	0	0	0	0	0
YCbCrtoRGB_C0_0	106	61	36	36	0	0	0	0	1	0	0	0	0	0
alpha_enable_0	0	8	0	0	0	0	0	0	0	0	0	0	0	0
apb3_if_0	31	50	0	0	0	0	0	0	0	0	0	0	0	0
delay_buffer_0	0	32	0	0	0	0	0	0	0	0	0	0	0	0
hist_ip_0	88	49	72	72	0	0	0	2	0	0	0	0	0	0
intensity_average_0	97	66	0	0	0	0	0	0	0	0	0	0	0	0
pip_mode_0	113	55	0	0	0	0	0	0	0	0	0	0	0	0
selector_0	4	0	0	0	0	0	0	0	0	0	0	0	0	0

2. Demo Requirements (Ask a Question)

The following table lists the hardware and software required for running the demo.

Table 2-1. Demo Requirements

Requirement	Description
Hardware and Accessories	
PolarFire® SoC video kit	MPFS250-VIDEO-KIT
Image Sensor module	LI-IMX334-MIPI-MICRO v1.0
USB A to Micro-USB B cable	Required for: • FPGA programming • UART interface with the Video Control GUI
HDMI cable	HDMI A male-to-male cable
HDMI monitor	To display the processed resultant video data for a full HD resolution (1920x1080)
Power adapter	12V, 5A
Host PC	A host PC with USB and Ethernet port
Utility Software	
FlashPro Express v2022.3	To program the job file on PolarFire SoC FPGA device
Programming job file	`PFSoC_VIDEO_PIP`

3. Demo Prerequisites (Ask a Question)

Before you start:

1. Download the design file from the following link: www.microchip.com/en-us/application-notes/AN4723
   The programming job file is placed at
   `<$download_directory>\mpfs_an4723_v2022p3_df\Programming_File`.
2. Download the Video Control GUI from: www.microchip.com/en-us/application-notes/AN4723

4. Installing the Video Control GUI (Ask a Question)

To install the Video Control GUI, follow these steps:

1. Extract the contents of the `mpfs_an4723_v2022p3_df.zip` file and run the `setup.exe` file from `mpfs_an4723_v2022p3_df/GUI/Video_Control_GUI_Installer/`.
2. Click **Yes** for any message from User Account Control. The **Video Control GUI** installation wizard is displayed.
3. Confirm the installation directory locations for the GUI and the National Instruments products and click **Next**.
4. Accept the license agreement and click **Next**.
5. Review the summary and click **Next**. The installation proceeds with a progress bar. After the installation, a confirmation message is displayed.
6. Click **Next** to exit the installation wizard.
7. Restart the host PC when prompted. The Video_Control GUI is installed.

© 2023 Microchip Technology Inc.
and its subsidiaries

5. Setting Up the Demo (Ask a Question)

The demonstration involves the following steps:

- 5.1. Setting Up the Hardware
- 5.2. Setting Up the Serial Terminal
- 5.3. Programming the Device

5.1 Setting Up the Hardware (Ask a Question)

Setting up the hardware involves interfacing the camera sensor module and the HDMI monitor with the PolarFire SoC video kit.

Follow these steps:

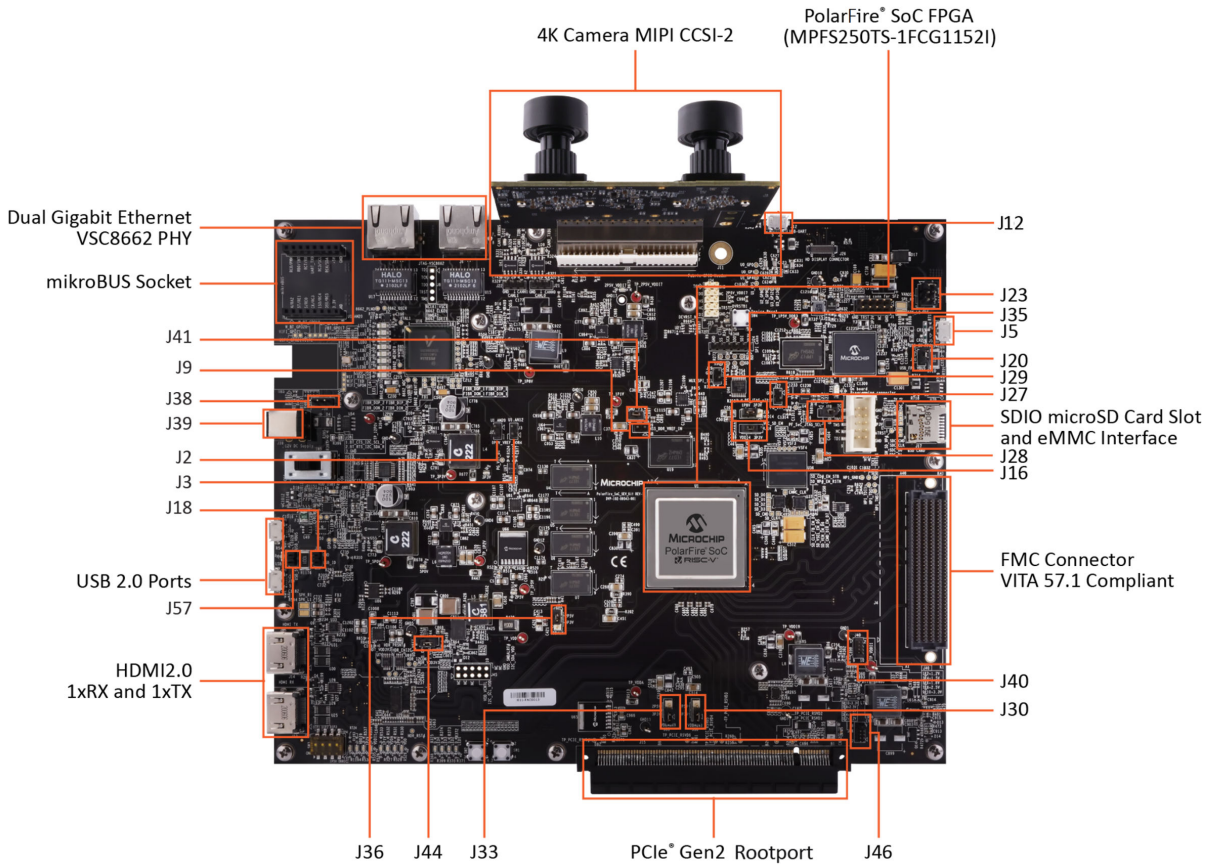
1. Connect the camera sensor module at **J10** on the video kit.
2. Connect the HDMI monitor at **J14** on the video kit using the HDMI cable.
3. Ensure that the jumper settings on the video kit are listed in the following table. For more information about the default jumper settings, see the “Jumper Settings” section in PolarFire SoC FPGA Video Kit User Guide.

Table 5-1. Jumper Settings

Jumper	Suggested Position	Functionality
J46	9 and 10	Bank 1 voltage for UART communication
J40	9 and 10	Bank 9 voltage
J2 and J3	Open	DDR4 ref voltage
J20	1 and 2	VBUS for FlashPro 6
J23	1 and 2	Backlight LED driver VANODE
J29	Open	External on-board SPI Flash
J27	Open	JTAG TRSTB
J39	12V Input	12V input to Board
J28	1 and 2	embedded Flash Programmer 6 (eFP6)
J41	1 and 2	MSS reference 125 MHz clock
J9	Open	MSS DDR Vref
J33	1 and 2	VDDAUX9 3.3V
J30	1 and 2	VDDAUX1 3.3V
J18	Open	USB ID
J57	Open	USB VBUS
J44	1 and 2	Core voltage 1.05V

The following figure shows the jumpers on the PolarFire SoC video kit.

Figure 5-1. Board Callout



5.2 Setting Up the Serial Terminal (Ask a Question)

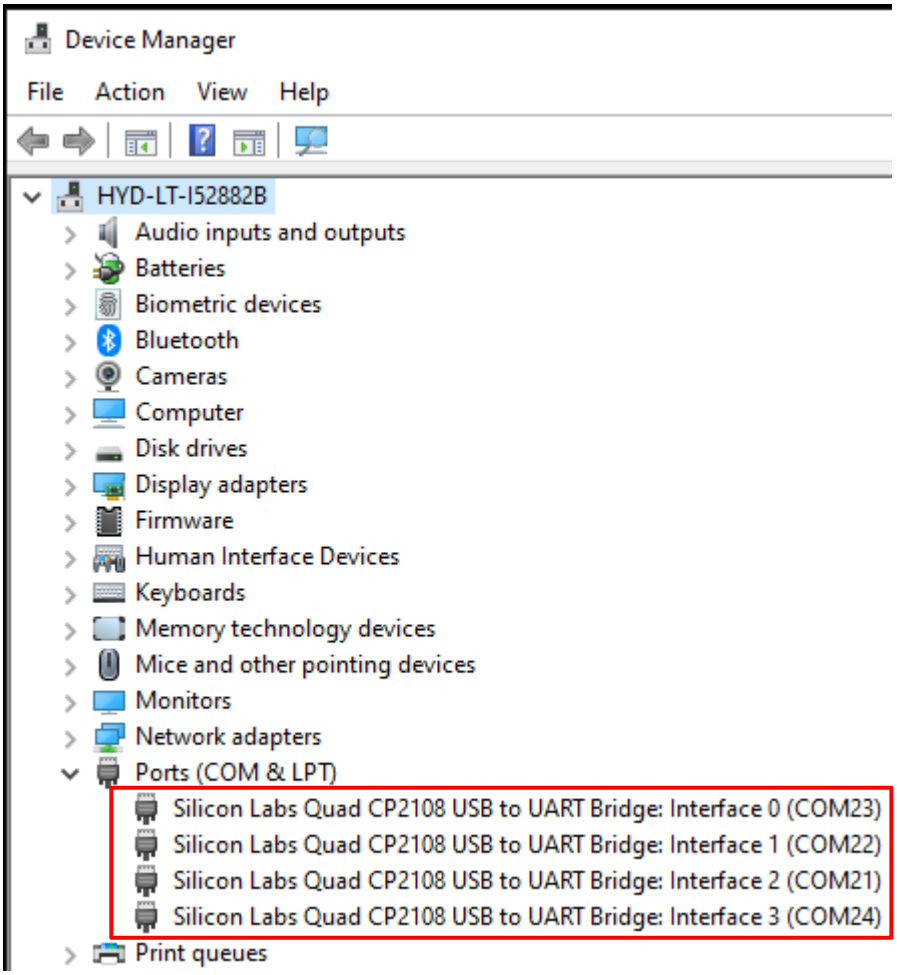
PolarFire SoC video kit includes CP2108 USB to establish communication between the video kit and host PC. Before you start:

- Download and install CP210x Universal Windows Driver.
- Unzip and see the *CP210x_Universal_Windows_Driver_ReleaseNotes*.

After installing the driver, follow these steps:

1. Connect USB cable at **J12** port on PolarFire SoC video kit board to the host PC.
2. After connecting power adapter to the board at **J39**, switch ON the power supply using the **SW5** switch. This must detect the USB UART chip on the board at the host PC. You can confirm this at the host PC device manager, see the following figure.

Figure 5-2. Device Manager



The Interface 0 COM port (COM23) is used to connect the Video Control GUI. The interface 0 might be on a different COM port number other than the ports shown in the preceding figure.

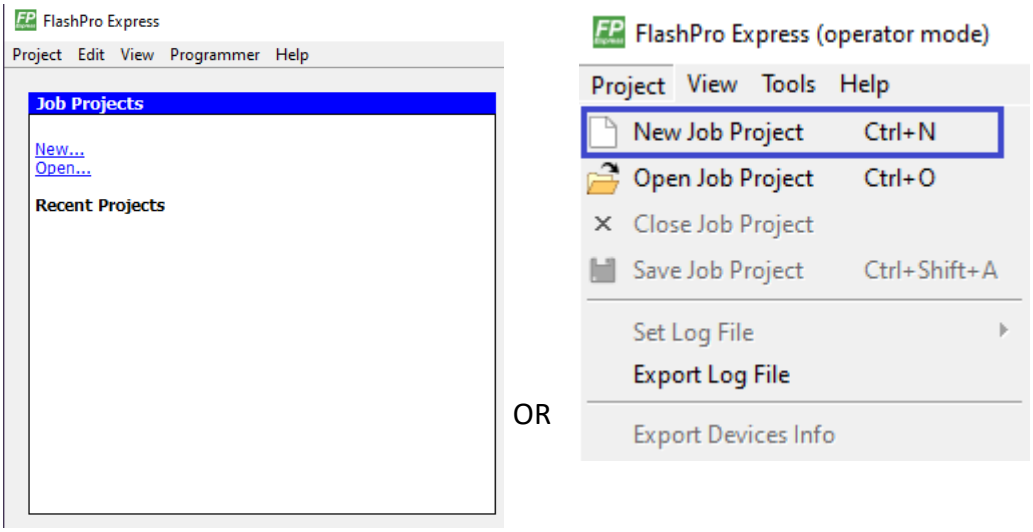
5.3 Programming the Device (Ask a Question)

This section describes the steps to program the PolarFire SoC device with the job file using FlashPro Express. The `PFSoC_VIDEO_PIP.job` file is available at `mpfs_an4723_v2022p3_df\Programming_File`.

Follow these steps:

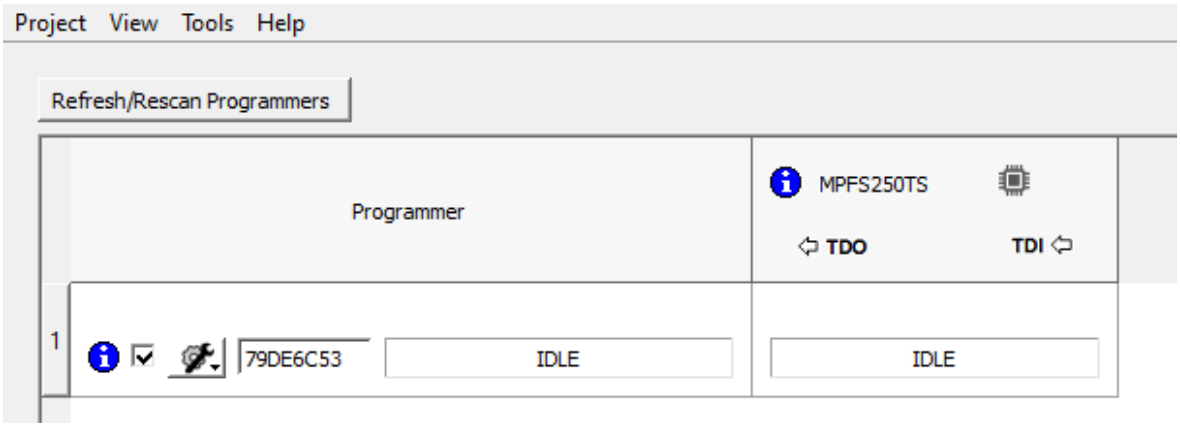
1. Connect a micro USB to **J5** from the host PC and start the FlashPro Express software from its installation directory.
2. Select **New** or **New Job Project** from the **Project** menu to create a new job project, see the following figure.

Figure 5-3. New FlashPro Express Project



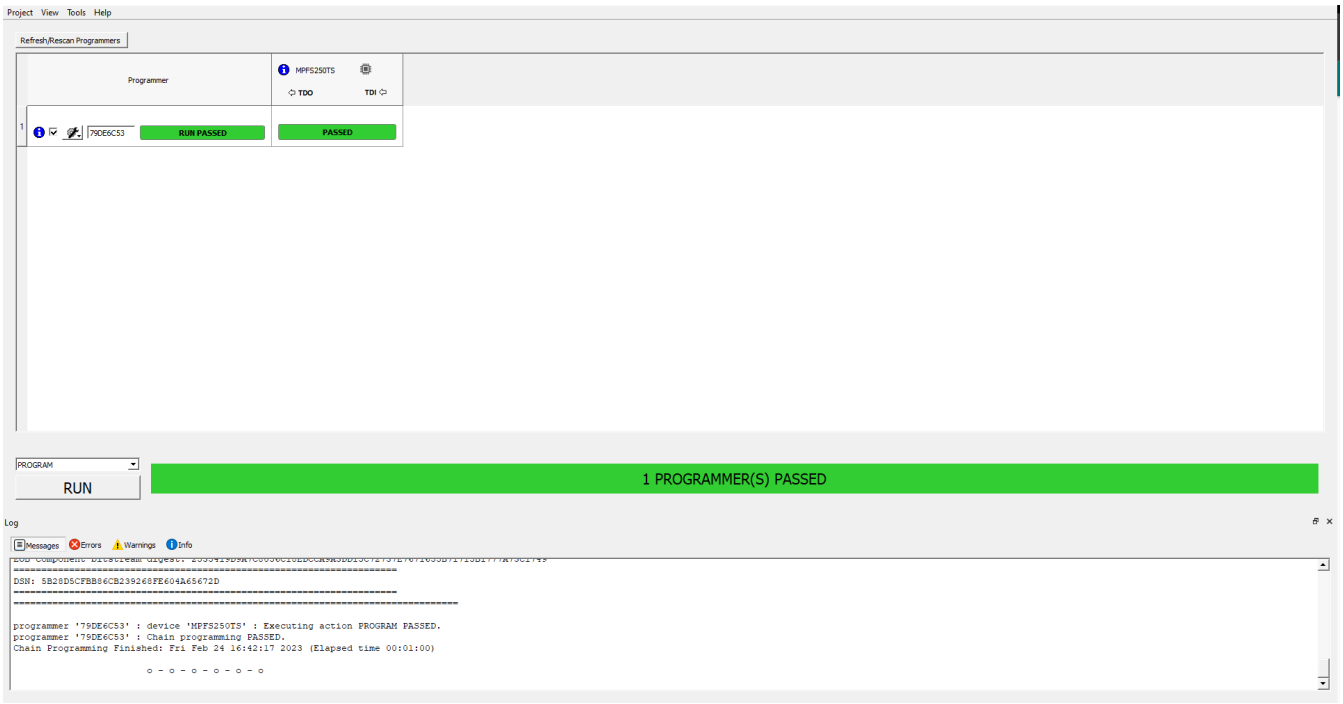
3. In the **New Job Project** dialog box, enter the following:
   - Programming job file: Click **Browse** and navigate to the location where the job file is located and select the file. The default location is `mpfs_an4723_v2022p3_df\Programming_File`.
   - FlashPro Express job project location: Select **Browse** and navigate to the location where you want to save the project.
4. Click **Open**. The required programming file is selected and ready to be programmed in the device. The FlashPro Express window appears. Confirm that a programmer number (for example, 79DE6C53) appears in the **Programmer** field as shown in the following figure. If it does not, check the board connections and click **Refresh/Rescan Programmers**.

   Figure 5-4. Programmer Number



5. Click **RUN** to program the device. When the device is programmed successfully, a RUN PASSED status is displayed as shown in the following figure.

Figure 5-5. RUN PASSED Status



6. Close FlashPro Express (**Project** > **Exit**).
7. Power-cycle the board using **SW5** switch.

6. Running the Demo (Ask a Question)

The demo features receiving the MIPI Rx data from two cameras with Full HD (FHD) resolution (1920x1080). The frames from a camera are stored in DDR4 memory and passed them onto the display as per the display controller timing parameters. The image processing pipeline on the display side uses bayer interpolation, gamma correction, histogram, edge detection, and image enhancement IPs to enhance the raw image from the camera. Also, the demo uses the automatic camera exposure control based on the lighting conditions. In the demo design, display controller is used to provide FHD video sync signals.

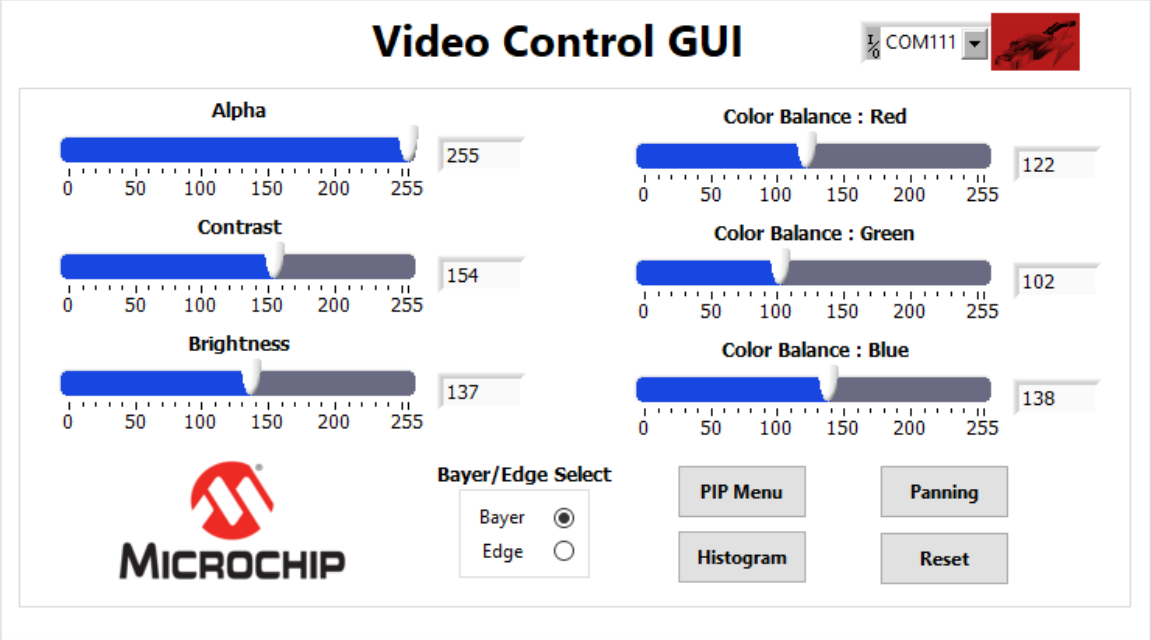
The FHD output supports PIP, edge detection, and image enhancements such as contrast, brightness, color balance, and alpha blending. The Video Control GUI for image enhancements is common for both the video outputs.

Running the demo involves verifying the imaging and video settings using the Video Control GUI and then observing the result on the HDMI monitor.

To use the demo GUI:

1. Launch the **Video_Control** GUI from the installation directory. The GUI is displayed, as shown in the following figure.

   Figure 6-1. Video Contol GUI



2. Select the Interface 0 (**COM23**) port as described in 5.2. Setting Up the Serial Terminal and select the **Connect** option. The **Connect** button turns green indicating a successful connection, as shown in Figure 6-3.

   Figure 6-2. Connecting the GUI and Video Kit

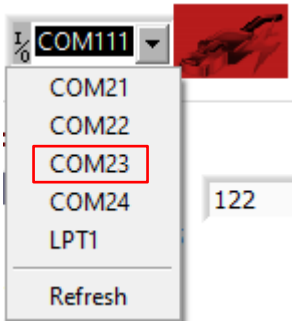
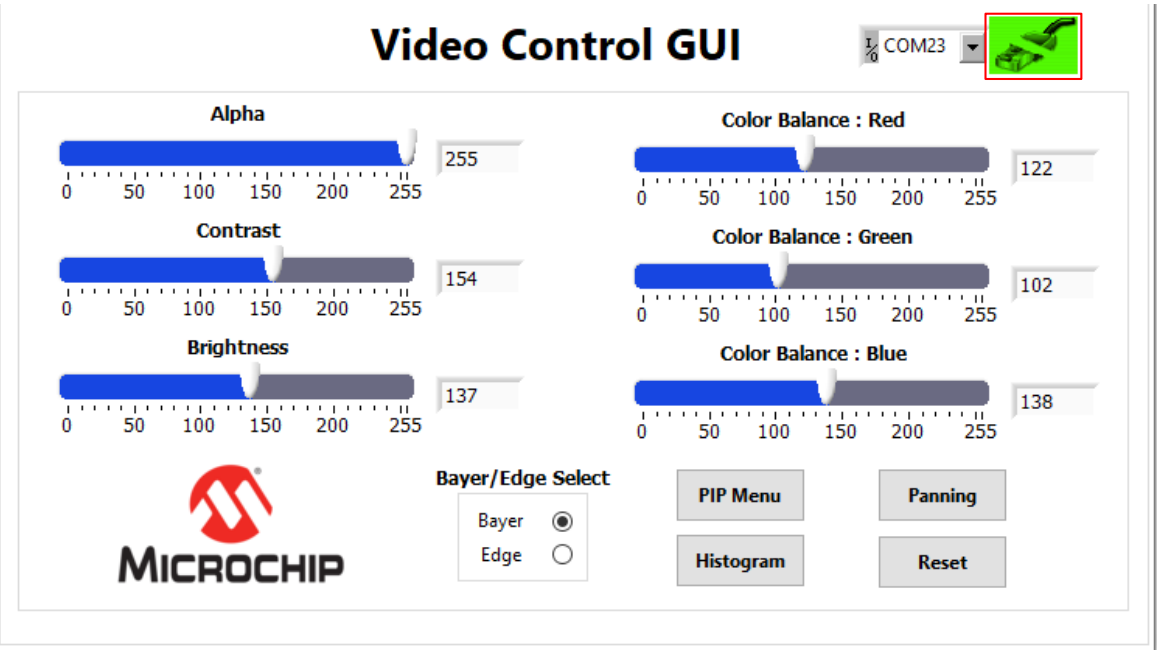
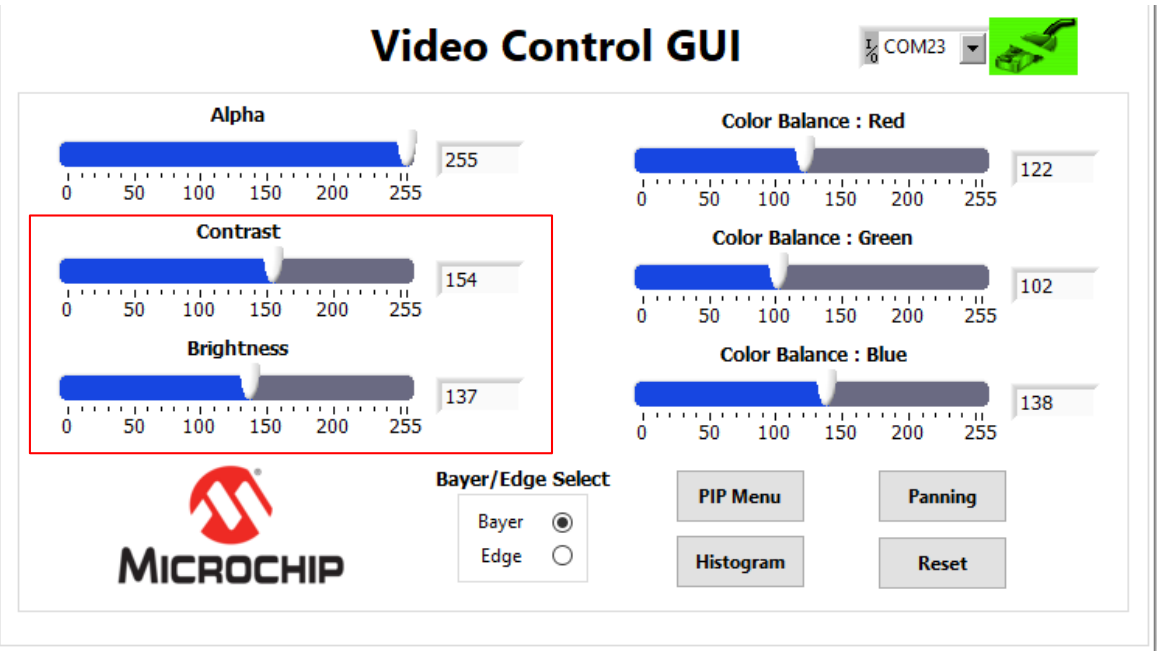


Figure 6-3. Connection Successful



3. Use the **Contrast** and **Brightness** sliders to adjust the contrast and brightness and observe the change on the HDMI monitor. The sliders are highlighted in the following figure.

Figure 6-4. Adjusting Contrast and Brightness

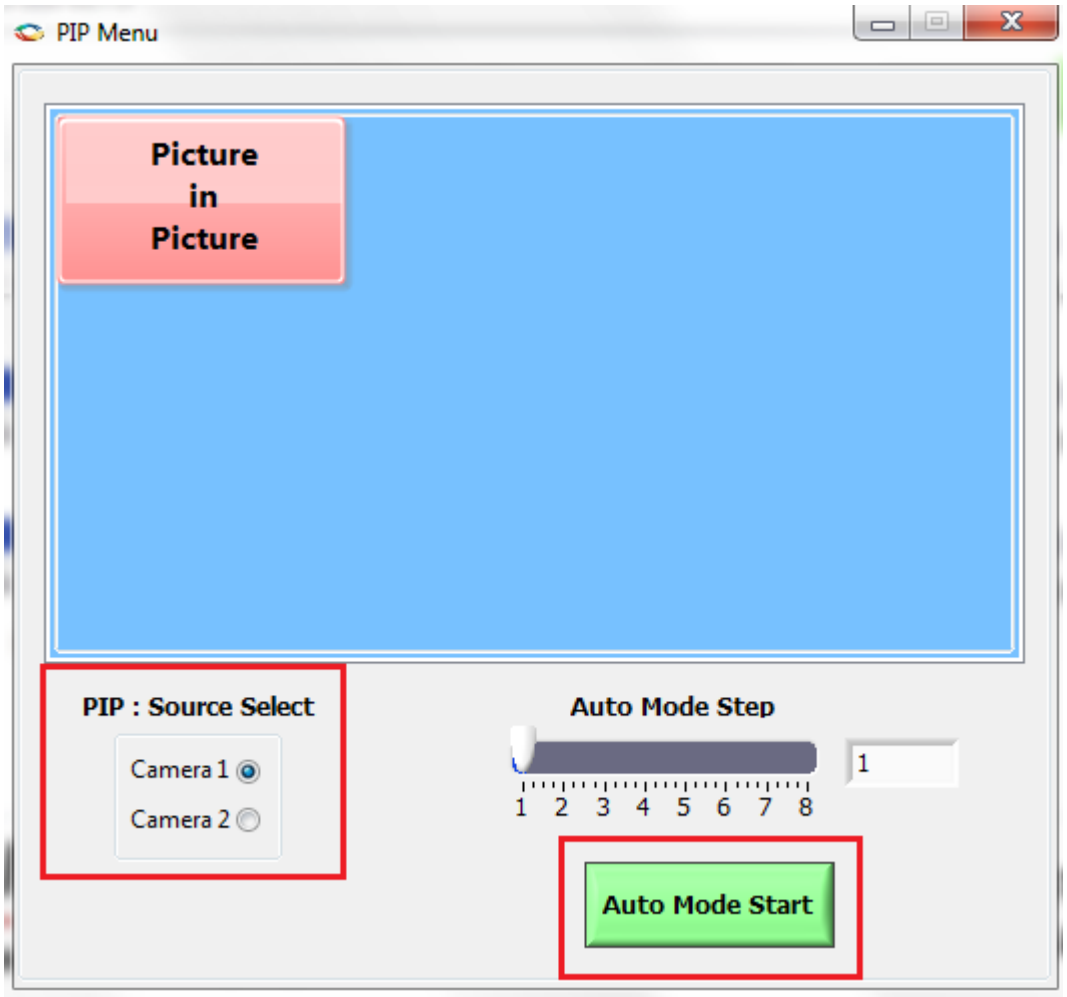


4. Similarly, adjust the color balance of the image using the color balance sliders.
5. Adjust the **Alpha** slider. The alpha blending feature enables adjusting the transparency of the PIP image. When the alpha value is adjusted to minimum (0), the image disappears.

Important: Revert to the default image settings by clicking the **Reset** option.

6. Click the **PIP Menu** to change the PIP settings.
7. Select the source of the PIP window between Camera 1 and Camera 2 using **PIP: Source Select**. The position of the PIP window can be moved anywhere within the screen by dragging the pink **Picture In Picture** box. The **Auto Mode Start** option moves the PIP window automatically. The speed of this movement can be controlled using the **Auto Mode Step** slider.

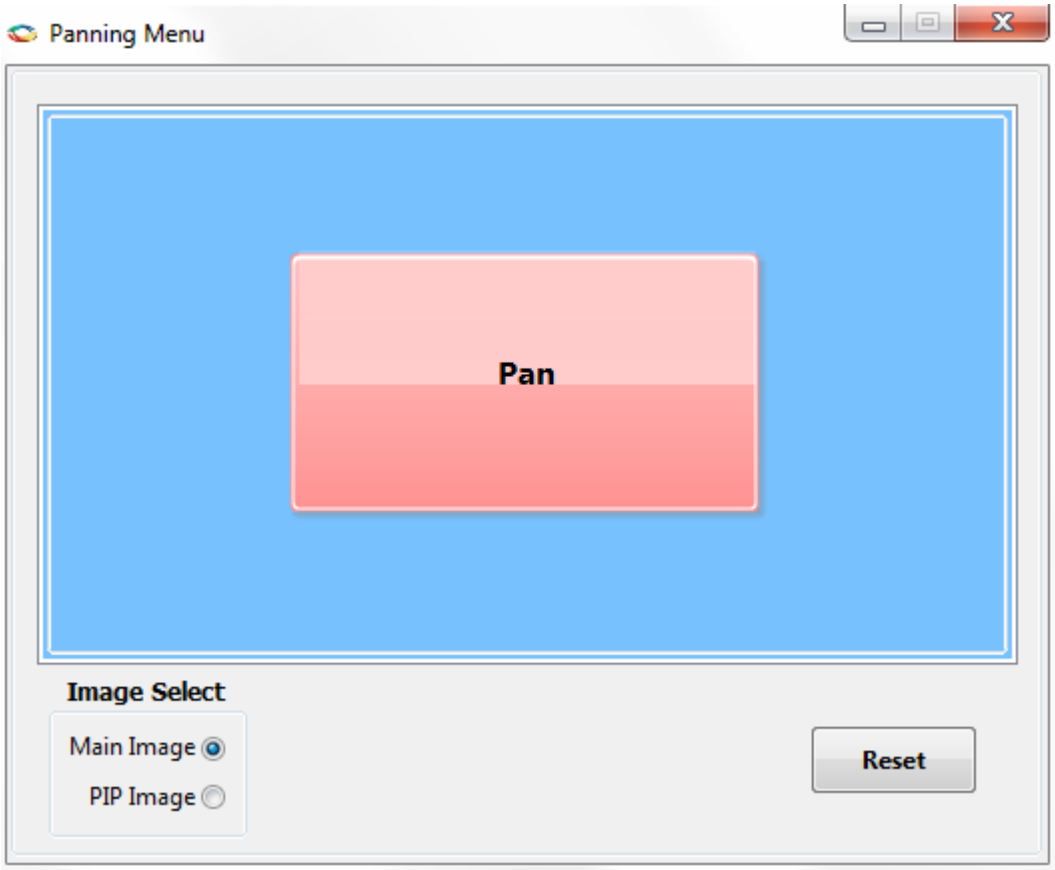
Figure 6-5. PIP Menu



8. Close the **PIP Menu** window.
9. In the main video control GUI window, select the **Panning** option to view a particular area of the main or the PIP image within a 4K image.
10. In the **Panning Menu** window, use **Image Select** to select the image to be panned (Main image or PIP image). Any area of the 4K camera feed can be viewed by dragging the pink box horizontally or vertically. The **Reset** option sets the view of the **Main Image** and **PIP Image** to its default center position.

© 2023 Microchip Technology Inc. and its subsidiaries

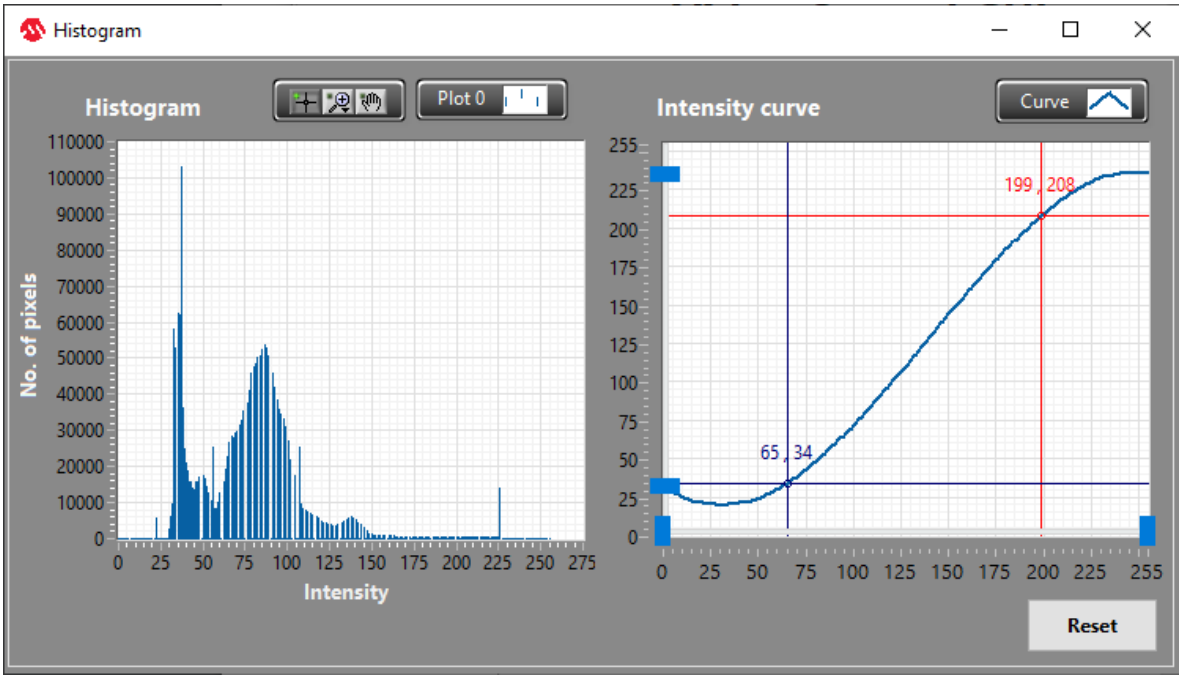
Figure 6-6. Panning Menu



11. Close the **Panning Menu** window to return to the main GUI.
12. In the main video control GUI window, click **Histogram** to view the histogram plot of the live video.
    The following histogram bar graph shows the number of pixels with a particular intensity level. For example, a y-axis value of 500000 at x-axis 100 indicates that there are 500000 pixels with an intensity of 100 (range is 0 to 255). The Intensity curve on the right side can be used to remap the intensity levels to a new value. The advantage of using intensity curve is that the pixels intensities can be remapped, independently. For example, the pixels below a range of intensity 50 can be modified, independently. The curve can also be used to adjust the black levels of the video frames.

© 2023 Microchip Technology Inc.
and its subsidiaries

Figure 6-7. Histogram



13. Close the **Histogram** window to return to the main GUI.
14. Close the GUI to exit from the demo.

This concludes the demo.

7. Appendix: Running the Tcl Script (Ask a Question)

Tcl scripts are provided in the design files folder under the `TCL_Scripts` directory.

To run Tcl, follow these steps:

1. Launch the Libero software.
2. Select **Project** > **Execute Script**.
3. Click **Browse** and select `PFSoC_Video_PIP.tcl` from the downloaded `TCL_Scripts` directory.
4. Click **Run**. After a successful execution of the Tcl script, the Libero project is created within the `TCL_Scripts` directory.

Important: Following arguments can be passed on to the Libero SoC tool while running the Tcl scripts:

- SYNTHESIZE: Runs synthesis after generating a design.
- PLACEROUTE: Runs synthesis and place and route after generating a design.
- VERIFY_TIMING: Runs required steps and timing verification after generating a design.
- GENERATE_BITSTREAM: Runs required steps and generates bit stream files to program the device after generating a design.
- PROGRAM: Runs the required steps and programs a connected device after generating a design.

See Tcl Commands Reference Guide for more information about Tcl commands. Contact Technical Support for any queries about running the Tcl script.

8. Revision History (Ask a Question)

The revision history table describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Revision	Date	Description
B	03/2023	• Replaced “SEV kit” with “video kit” throughout the document. • Updated for Libero SoC v2022.3 release.
A	08/2022	Initial Revision

Microchip FPGA Support (Ask a Question)

Microchip FPGA products group backs its products with various support services, including Customer Service, Customer Technical Support Center, a website, and worldwide sales offices. Customers are suggested to visit Microchip online resources prior to contacting support as it is very likely that their queries have been already answered.

Contact Technical Support Center through the website at www.microchip.com/support. Mention the FPGA Device Part number, select appropriate case category, and upload design files while creating a technical support case.

Contact Customer Service for non-technical product support, such as product pricing, product upgrades, update information, order status, and authorization.

- From North America, call **800.262.1060**
- From the rest of the world, call **650.318.4460**
- Fax, from anywhere in the world, **650.318.8044**

Microchip Information (Ask a Question)

The Microchip Website (Ask a Question)

Microchip provides online support via our website at www.microchip.com/. This website is used to make files and information easily available to customers. Some of the content available includes:

- **Product Support** – Data sheets and errata, application notes and sample programs, design resources, user's guides and hardware support documents, latest software releases and archived software
- **General Technical Support** – Frequently Asked Questions (FAQs), technical support requests, online discussion groups, Microchip design partner program member listing
- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

Product Change Notification Service (Ask a Question)

Microchip's product change notification service helps keep customers current on Microchip products. Subscribers will receive email notification whenever there are changes, updates, revisions or errata related to a specified product family or development tool of interest.

To register, go to www.microchip.com/pcn and follow the registration instructions.

Customer Support (Ask a Question)

Users of Microchip products can receive assistance through several channels:

- Distributor or Representative
- Local Sales Office
- Embedded Solutions Engineer (ESE)
- Technical Support

Customers should contact their distributor, representative or ESE for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in this document.

Technical support is available through the website at: www.microchip.com/support

Microchip Devices Code Protection Feature (Ask a Question)

Note the following details of the code protection feature on Microchip products:

© 2023 Microchip Technology Inc. and its subsidiaries

- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is secure when used in the intended manner, within operating specifications, and under normal conditions.
- Microchip values and aggressively protects its intellectual property rights. Attempts to breach the code protection features of Microchip product is strictly prohibited and may violate the Digital Millennium Copyright Act.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of its code. Code protection does not mean that we are guaranteeing the product is “unbreakable”. Code protection is constantly evolving. Microchip is committed to continuously improving the code protection features of our products.

Legal Notice (Ask a Question)

This publication and the information herein may be used only with Microchip products, including to design, test, and integrate Microchip products with your application. Use of this information in any other manner violates these terms. Information regarding device applications is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. Contact your local Microchip sales office for additional support or, obtain additional support at www.microchip.com/en-us/support/design-help/client-support-services.

THIS INFORMATION IS PROVIDED BY MICROCHIP "AS IS". MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION INCLUDING BUT NOT LIMITED TO ANY IMPLIED WARRANTIES OF NON-INFRINGEMENT, MERCHANTABILITY, AND FITNESS FOR A PARTICULAR PURPOSE, OR WARRANTIES RELATED TO ITS CONDITION, QUALITY, OR PERFORMANCE.

IN NO EVENT WILL MICROCHIP BE LIABLE FOR ANY INDIRECT, SPECIAL, PUNITIVE, INCIDENTAL, OR CONSEQUENTIAL LOSS, DAMAGE, COST, OR EXPENSE OF ANY KIND WHATSOEVER RELATED TO THE INFORMATION OR ITS USE, HOWEVER CAUSED, EVEN IF MICROCHIP HAS BEEN ADVISED OF THE POSSIBILITY OR THE DAMAGES ARE FORESEEABLE. TO THE FULLEST EXTENT ALLOWED BY LAW, MICROCHIP'S TOTAL LIABILITY ON ALL CLAIMS IN ANY WAY RELATED TO THE INFORMATION OR ITS USE WILL NOT EXCEED THE AMOUNT OF FEES, IF ANY, THAT YOU HAVE PAID DIRECTLY TO MICROCHIP FOR THE INFORMATION.

Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights unless otherwise stated.

Trademarks (Ask a Question)

The Microchip name and logo, the Microchip logo, Adaptec, AVR, AVR logo, AVR Freaks, BesTime, BitCloud, CryptoMemory, CryptoRF, dsPIC, flexPWR, HELDO, IGLOO, JukeBlox, KeeLoq, Kleer, LANCheck, LinkMD, maXStylus, maXTouch, MediaLB, megaAVR, Microsemi, Microsemi logo, MOST, MOST logo, MPLAB, OptoLyzer, PIC, picoPower, PICSTART, PIC32 logo, PolarFire, Prochip Designer, QTouch, SAM-BA, SenGenuity, SpyNIC, SST, SST Logo, SuperFlash, Symmetricom, SyncServer, Tachyon, TimeSource, tinyAVR, UNI/O, Vectron, and XMEGA are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

AgileSwitch, APT, ClockWorks, The Embedded Control Solutions Company, EtherSynch, Flashtec, Hyper Speed Control, HyperLight Load, Libero, motorBench, mTouch, Powermite 3, Precision Edge, ProASIC, ProASIC Plus, ProASIC Plus logo, Quiet- Wire, SmartFusion, SyncWorld, Temux, TimeCesium, TimeHub, TimePictra, TimeProvider, TrueTime, and ZL are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Adjacent Key Suppression, AKS, Analog-for-the-Digital Age, Any Capacitor, AnyIn, AnyOut, Augmented Switching, BlueSky, BodyCom, Clockstudio, CodeGuard, CryptoAuthentication, CryptoAutomotive, CryptoCompanion, CryptoController, dsPICDEM, dsPICDEM.net, Dynamic Average Matching, DAM, ECAN, Espresso T1S, EtherGREEN, GridTime, IdealBridge, In-Circuit Serial Programming, ICSP, INICnet, Intelligent Paralleling, IntelliMOS, Inter-Chip Connectivity, JitterBlocker, Knob-on-Display, KoD, maxCrypto, maxView, memBrain, Mindi, MiWi, MPASM, MPF, MPLAB Certified logo, MPLIB, MPLINK, MultiTRAK, NetDetach, Omniscient Code Generation, PICDEM, PICDEM.net, PICkit, PICtail, PowerSmart, PureSilicon, QMatrix, REAL ICE, Ripple Blocker, RTAX, RTG4, SAM-

ICE, Serial Quad I/O, simpleMAP, SimpliPHY, SmartBuffer, SmartHLS, SMART-I.S., storClad, SQI, SuperSwitcher, SuperSwitcher II, Switchtec, SynchroPHY, Total Endurance, Trusted Time, TSHARC, USBCheck, VariSense, VectorBlox, VeriPHY, ViewSpan, WiperLock, XpressConnect, and ZENA are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

The Adaptec logo, Frequency on Demand, Silicon Storage Technology, and Symmcom are registered trademarks of Microchip Technology Inc. in other countries.

GestIC is a registered trademark of Microchip Technology Germany II GmbH & Co. KG, a subsidiary of Microchip Technology Inc., in other countries.

All other trademarks mentioned herein are property of their respective companies.

© 2023, Microchip Technology Incorporated and its subsidiaries. All Rights Reserved.

ISBN: 978-1-6683-2216-1

Quality Management System (Ask a Question)

For information regarding Microchip's Quality Management Systems, please visit www.microchip.com/quality.

Worldwide Sales and Service

AMERICAS	ASIA/PACIFIC	ASIA/PACIFIC	EUROPE
Corporate Office 2355 West Chandler Blvd. Chandler, AZ 85224-6199 Tel: 480-792-7200 Fax: 480-792-7277 Technical Support: www.microchip.com/support Web Address: www.microchip.com **Atlanta** Duluth, GA Tel: 678-957-9614 Fax: 678-957-1455 **Austin, TX** Tel: 512-257-3370 **Boston** Westborough, MA Tel: 774-760-0087 Fax: 774-760-0088 **Chicago** Itasca, IL Tel: 630-285-0071 Fax: 630-285-0075 **Dallas** Addison, TX Tel: 972-818-7423 Fax: 972-818-2924 **Detroit** Novi, MI Tel: 248-848-4000 **Houston, TX** Tel: 281-894-5983 **Indianapolis** Noblesville, IN Tel: 317-773-8323 Fax: 317-773-5453 Tel: 317-536-2380 **Los Angeles** Mission Viejo, CA Tel: 949-462-9523 Fax: 949-462-9608 Tel: 951-273-7800 **Raleigh, NC** Tel: 919-844-7510 **New York, NY** Tel: 631-435-6000 **San Jose, CA** Tel: 408-735-9110 Tel: 408-436-4270 **Canada - Toronto** Tel: 905-695-1980 Fax: 905-695-2078	**Australia - Sydney** Tel: 61-2-9868-6733 **China - Beijing** Tel: 86-10-8569-7000 **China - Chengdu** Tel: 86-28-8665-5511 **China - Chongqing** Tel: 86-23-8980-9588 **China - Dongguan** Tel: 86-769-8702-9880 **China - Guangzhou** Tel: 86-20-8755-8029 **China - Hangzhou** Tel: 86-571-8792-8115 **China - Hong Kong SAR** Tel: 852-2943-5100 **China - Nanjing** Tel: 86-25-8473-2460 **China - Qingdao** Tel: 86-532-8502-7355 **China - Shanghai** Tel: 86-21-3326-8000 **China - Shenyang** Tel: 86-24-2334-2829 **China - Shenzhen** Tel: 86-755-8864-2200 **China - Suzhou** Tel: 86-186-6233-1526 **China - Wuhan** Tel: 86-27-5980-5300 **China - Xian** Tel: 86-29-8833-7252 **China - Xiamen** Tel: 86-592-2388138 **China - Zhuhai** Tel: 86-756-3210040	**India - Bangalore** Tel: 91-80-3090-4444 **India - New Delhi** Tel: 91-11-4160-8631 **India - Pune** Tel: 91-20-4121-0141 **Japan - Osaka** Tel: 81-6-6152-7160 **Japan - Tokyo** Tel: 81-3-6880- 3770 **Korea - Daegu** Tel: 82-53-744-4301 **Korea - Seoul** Tel: 82-2-554-7200 **Malaysia - Kuala Lumpur** Tel: 60-3-7651-7906 **Malaysia - Penang** Tel: 60-4-227-8870 **Philippines - Manila** Tel: 63-2-634-9065 **Singapore** Tel: 65-6334-8870 **Taiwan - Hsin Chu** Tel: 886-3-577-8366 **Taiwan - Kaohsiung** Tel: 886-7-213-7830 **Taiwan - Taipei** Tel: 886-2-2508-8600 **Thailand - Bangkok** Tel: 66-2-694-1351 **Vietnam - Ho Chi Minh** Tel: 84-28-5448-2100	**Austria - Wels** Tel: 43-7242-2244-39 Fax: 43-7242-2244-393 **Denmark - Copenhagen** Tel: 45-4485-5910 Fax: 45-4485-2829 **Finland - Espoo** Tel: 358-9-4520-820 **France - Paris** Tel: 33-1-69-53-63-20 Fax: 33-1-69-30-90-79 **Germany - Garching** Tel: 49-8931-9700 **Germany - Haan** Tel: 49-2129-3766400 **Germany - Heilbronn** Tel: 49-7131-72400 **Germany - Karlsruhe** Tel: 49-721-625370 **Germany - Munich** Tel: 49-89-627-144-0 Fax: 49-89-627-144-44 **Germany - Rosenheim** Tel: 49-8031-354-560 **Israel - Ra'anana** Tel: 972-9-744-7705 **Italy - Milan** Tel: 39-0331-742611 Fax: 39-0331-466781 **Italy - Padova** Tel: 39-049-7625286 **Netherlands - Drunen** Tel: 31-416-690399 Fax: 31-416-690340 **Norway - Trondheim** Tel: 47-72884388 **Poland - Warsaw** Tel: 48-22-3325737 **Romania - Bucharest** Tel: 40-21-407-87-50 **Spain - Madrid** Tel: 34-91-708-08-90 Fax: 34-91-708-08-91 **Sweden - Gothenberg** Tel: 46-31-704-60-40 **Sweden - Stockholm** Tel: 46-8-5090-4654 **UK - Wokingham** Tel: 44-118-921-5800 Fax: 44-118-921-5820

© 2023 Microchip Technology Inc.
and its subsidiaries