Software Defined Radio

AN5014

Introduction (Ask a Question)

A Software-Defined Radio (SDR) is a communication system that utilizes a programmable medium to implement radio components like mixers, filters, modulators/demodulators, and detection circuits. This approach offers enhanced flexibility and capabilities in the system.

A well-designed Software-Defined Radio (SDR) typically comprises various fixed components, such as an antenna, front-end RF hardware, and an ADC or DAC. The remaining functionalities are implemented in a programmable medium, referred to as "soft" components. While general-purpose processors are commonly used for this purpose, they often lack the required I/O bandwidth and processing capabilities, except for the most basic SDR architectures. FPGA systems fulfill the demands of complex SDR implementations by offering both the necessary I/O bandwidth and processing capabilities.

This demonstration outlines an SDR application on the PolarFire® FPGA. Baseband processing is implemented on the FPGA and transmitted using a wideband RF transceiver, AD9371. The transceiver is configured via a soft Mi-V processor on the PolarFire FPGA.

This design demonstrates the following features:

- Supports Wireless transmission of text or image files between two hardware setups
- Supports the UART GUI to transmit and receive the data
- Supports configuration of the AD9371 RF board using the Mi-V soft processor on FPGA device
- Provides carrier frequency and phase offset correction using Costas loop
- Supports FEC encoding to correct data transmission errors
- Supports Symbol Timing Synchronization
- Supports Custom Packetization and Depacketization Method
- Supports configurable parameters for wide range blocks

The demo includes a user-friendly SDR Graphical User Interface (GUI) to configure transmit and receive data.

The Microchip PolarFire FPGA Evaluation Kit (MPF300-EVAL-KIT), which is RoHS-compliant, enables you to evaluate the PolarFire family of FPGAs with support for the following interfaces:

- PCI Express Gen1 and Gen2
- 1 GbE
- DDR3 and DDR4 memory
- FMC HPC with eight transceiver lanes
- One full-duplex Transceiver SMAs
- SFP+ Cage
- UART interface to FTDI device
- SPI interface to SPI Flash device

For more information about the PolarFire Evaluation kit, see PolarFire FPGA Evaluation Kit.

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1. Demo Requirements (Ask a Question)

The following table lists the hardware and software required for running the demo.

Table 1-1. Demo Requirements

Requirement	Description
Hardware and Accessories	
PolarFire evaluation kit	MPF300-EVAL-KIT Two for two board demo and one for one board demo
USB A to Micro-USB B cable	Required for: • FPGA programming • UART interface with the Wireless Demo GUI
SMA cable	Female to Female Required for providing the reference clock from evaluation kit to AD9528 on the AD9371 FMC card
AD9371	Analog device's RF board for transceiver functionality and for digital signal processing function Two for two board demo and one for one board demo
Host PC	A host PC with USB port Two for two board demo and one for one board demo
Power adapter	12V and 5A Two for two board demo and one for one board demo
Omnidirectional antenna	Required for transmitting or receiving the radio signal Two (One for transmitting and other for receiving)
Utility Software	
FlashPro Express v2023.1	To program the job file on PolarFire® SoC FPGA device
Programming job file	`PFEval_SDR`

2. Demo Prerequisites (Ask a Question)

Before you start the demo, ensure that the following components are in place:

1. Download the design file from the following link: The programming job file is placed at `<$download_directory>\mpf_an5014_v2023p1_eval_df\Programming_File`
2. For demo design files download link: www.microchip.com/en-us/application-notes/AN5014

3. Demo Design (Ask a Question)

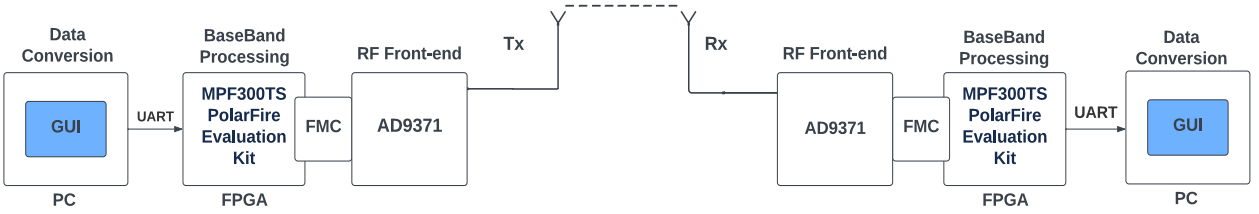
The Libero design contains both the transmitter (Tx) path and receiver (Rx) path. The communication with the analog radio chip, AD9371, happens through JESD 204B. As the design has both transmitter and receiver paths, the demo is operated in the following two modes:

1. Two boards communication
2. Same board communication

3.1 Two Boards Communication Setup (Ask a Question)

This setup requires two PolarFire FPGA Evaluation kits, two AD9371 FMC cards, and two PCs to run the demo. Setting up the demo is described in 5. Setting Up the Demo section. The user data received from the GUI is transmitted over the air from the transmitter setup and is received at the receiver setup. The received radio data is demodulated and processed to extract the user data and is displayed on the GUI connected to the receiver setup.

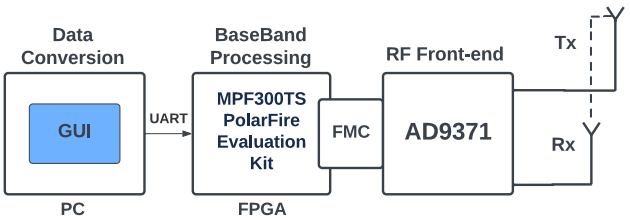
Figure 3-1. Two Boards Communication



3.2 Same Board Communication Setup (Ask a Question)

This setup requires one PolarFire FPGA Evaluation kit, one AD9371 FMC card and a PC to run the demo. The user data received from GUI is transmitted over the air and is received by the receiver on the same AD9371 FMC card. The received data is processed and displayed on the Receiver (Rx) tab of the same GUI that is used to send the user data.

Figure 3-2. Same Board Communication

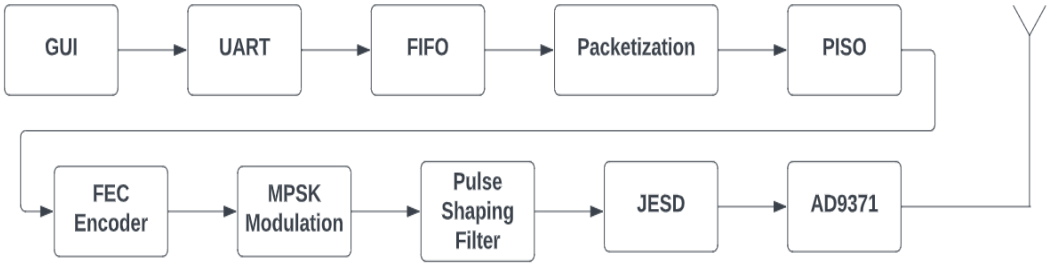


3.3 Transmitter (Ask a Question)

The data to be transmitted is entered in the UART based Graphical User Interface (GUI) in the form of a text message or the text data is chosen from a text file. Each maximum SDR packet length is defined as 1024 Bytes. If the message is greater than 1024 Bytes, then the message is divided into chunks of 1024 Bytes data. The message is passed to FPGA through UART Interface and is stored in a FIFO. Once a complete packet is written into FIFO, the SDR packet is created by appending 64 Bytes access code and 2 Bytes of Packet length at the start of the packet. Final data transmitted from the packetization is 64 Bytes of access code + 2 Bytes of Packet Length + n Bytes of message (n is the size of the packet and is limited to 1024).

From Packetization, the message is further serialized from byte to bit in Parallel In Serial Out (PISO). Transformed bit data is further encoded using FEC Encoder with code rate of 1/2 to minimize the bit errors while transmitting in a noisy environment. The encoded data is modulated into Quadrature Phase Shift Keying (QPSK) constellation and then passed through the pulse shaping filter, which reduces the Inter Symbol Interference (ISI) and adjacent channel interference. Pulse shaped data is sent to AD9371 using JESD Interface. From AD9371, the data is transmitted through wireless medium to the receiver.

Figure 3-3. Process Flow in Transmitter

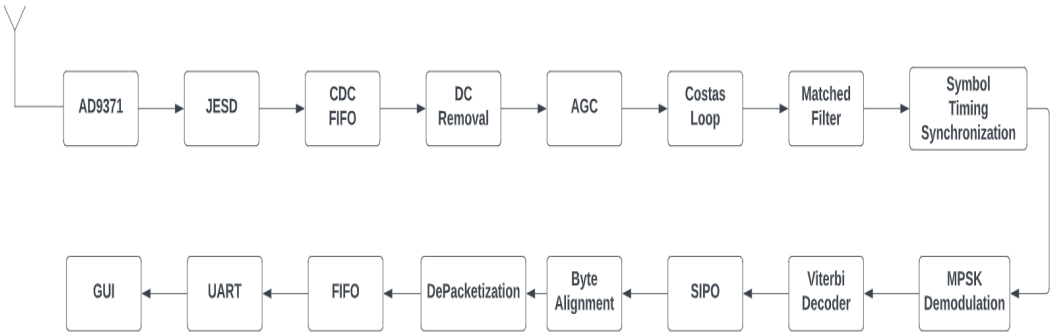


3.4 Receiver (Ask a Question)

The signal is received from the wireless medium and sent to the FPGA through AD9371 using the JESD interface at the receiver. The signal is further processed in the FPGA to recover the transmitted message or data and the incoming data from the JESD is stored in the FIFO. The DC removal block reads the data from the FIFO and removes the DC offset, which is then amplified in the AGC. The Costas loop (closed loop) is used to remove the phase offset. A Cascaded Integrator-Comb (CIC) filter decimated the phase and frequency corrected signal. Symbol Timing Synchronisation is used to find the optimal sampling instance of the filtered signal.

The MPSK demodulation block demodulates the data and is decoded in the Viterbi decoder. SIPO collects the bit data and converts it into byte data. The received data contains the access code and packet length, which need to be matched at depacketization and the data is separated from the packet structure and stored in a FIFO. The data is read from the FIFO through the UART interface and displayed in the GUI at the receiver end.

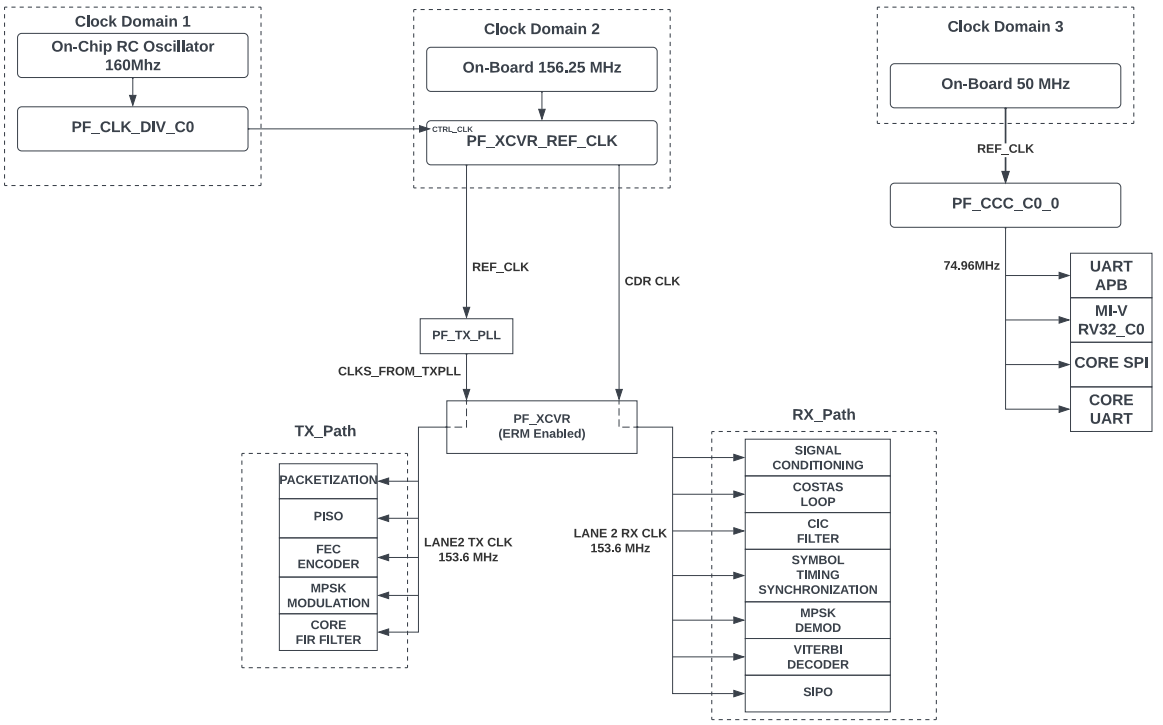
Figure 3-4. Process Flow in Receiver



3.5 Clocking Structure (Ask a Question)

The following figure shows the clocking structure of the design. PF_CCC_C0 generates the 50 MHz fabric clocks from the REF_CLK generated by PF_XCVR_REF_CLK. The on-board 156.25 MHz clock is the reference clock for the XCVR, which further provides the operating clock of 153.6 MHz for the TX_Path and RX_Path blocks.

Figure 3-5. Clocking Structure

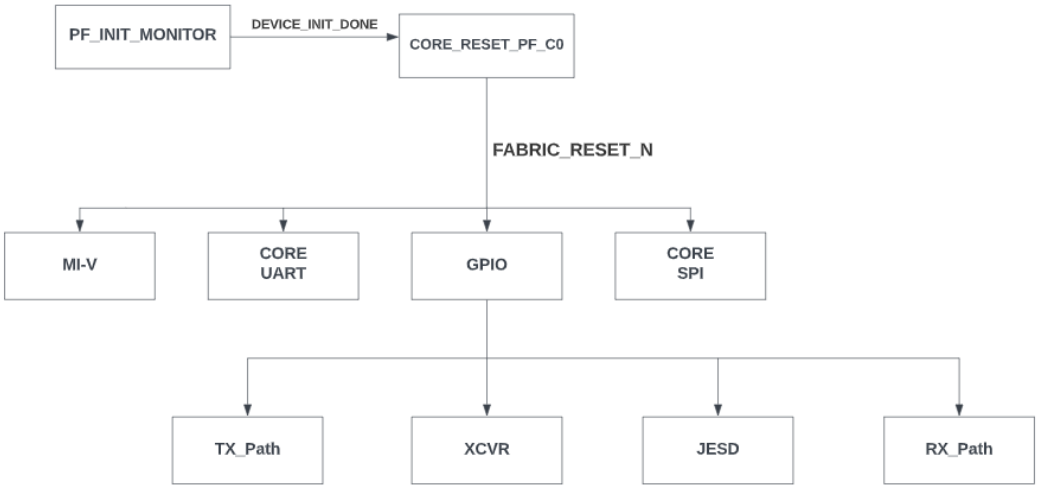


3.6 Reset Structure (Ask a Question)

The following figure shows the reset structure of the demo design. The INIT_MONITOR IP asserts the following signals:

- FABRIC_POR_N: Asserted after the initialization of the fabric and this signal is used to reset the Mi-V and respective blocks.
- DEVICE_INIT_DONE: Asserted after the initialization of the PolarFire device.

Figure 3-6. Reset Structure



3.7 Resource Utilization and Performance (Ask a Question)

A summary of SDR resource utilization and performance data is shown in following figure.

Figure 3-7. SDR Device Resource Utilization and Performance

Module Name	Fabric 4LUT	Fabric DFF	Interface 4LUT	Interface DFF	Single-Ended I/O	Differential I/O Pairs	uSRAM 1K	LSRAM 18K	Math (18x18)	Chip Globals	Row Global	PLL	Transceiver Lanes
Top	21492	15284	26220	26220	26	3	46	669	44	14	9	3	5
Primitives	1	0	0	0	26	0	0	0	0	0	0	0	0
Proc_Sub_System_inst_0	8698	3452	19392	19392	0	0	8	536	0	5	0	1	0
SDR_inst_0	8479	7026	2292	2292	0	3	38	7	44	6	8	2	4
Primitives	2	0	0	0	0	1	0	0	0	0	0	0	0
JESD_0	3236	2867	384	384	0	2	32	0	0	2	8	0	4
RX_Path_inst_0	4349	3237	600	600	0	0	2	6	10	3	0	1	0
Primitives	2	0	0	0	0	0	0	0	0	2	0	0	0
BYTE_ALLIGNMEN...	77	36	0	0	0	0	0	0	0	0	0	0	0
CDC_video_fifo_0	69	88	72	72	0	0	0	2	0	0	0	0	0
CORECIC_C0_I	313	765	0	0	0	0	0	0	0	0	0	0	0
CORECIC_C0_Q	296	753	0	0	0	0	0	0	0	0	0	0	0
COREFIFO_C1_0	142	164	36	36	0	0	0	1	0	0	0	0	0
MPSK_Demod_C0_0	16	8	0	0	0	0	0	0	0	0	0	0	0
PF_CCC_C3_0	0	0	0	0	0	0	0	0	0	1	0	1	0
SIGNAL_Condition...	1351	620	144	144	0	0	0	0	4	0	0	0	0
AGC_inst_0	829	339	144	144	0	0	0	0	4	0	0	0	0
DC_Removal_I	83	73	0	0	0	0	0	0	0	0	0	0	0
DC_Removal_Q	69	63	0	0	0	0	0	0	0	0	0	0	0
IQ_MAG_AVG_0	370	145	0	0	0	0	0	0	0	0	0	0	0
SIPO_0	24	34	0	0	0	0	0	0	0	0	0	0	0
Viterbi_Decoder_C...	298	225	108	108	0	0	0	3	0	0	0	0	0
costas_top_C1_0	1269	217	216	216	0	0	0	0	6	0	0	0	0
depacketization_0	120	56	0	0	0	0	0	0	0	0	0	0	0
read_fifo_logic_0	8	16	0	0	0	0	0	0	0	0	0	0	0
timing_sync_0	357	255	24	24	0	0	2	0	0	0	0	0	0
xor20bit_0	7	0	0	0	0	0	0	0	0	0	0	0	0
STATUS_LED_0	6	8	0	0	0	0	0	0	0	0	0	0	0
TX_Path_inst_0	751	578	1308	1308	0	0	4	1	34	1	0	1	0
Primitives	1	0	0	0	0	0	0	0	0	0	0	0	0
COREFIFO_C0_0	144	156	36	36	0	0	0	1	0	0	0	0	0
DATA_RATE_GENER...	46	35	0	0	0	0	0	0	0	0	0	0	0
FEC_Encoder_C0_0	3	9	0	0	0	0	0	0	0	0	0	0	0
GUARD_Band_SIG_...	98	85	0	0	0	0	0	0	0	0	0	0	0
MUX_IQ_VLD_0	44	47	0	0	0	0	0	0	0	0	0	0	0
PISO_1	54	38	0	0	0	0	0	0	0	0	0	0	0
Interpolator_Block_0	97	125	1272	1272	0	0	4	0	34	0	0	0	0
COREFIR_PF_C...	31	34	636	636	0	0	2	0	17	0	0	0	0
COREFIR_PF_C...	32	41	636	636	0	0	2	0	17	0	0	0	0
UPSampling	34	50	0	0	0	0	0	0	0	0	0	0	0
MPSK_Mod_C0_0	47	32	0	0	0	0	0	0	0	0	0	0	0
MSC_i_9	47	32	0	0	0	0	0	0	0	0	0	0	0
PF_CCC_C1_0	0	0	0	0	0	0	0	0	0	1	0	1	0
PISO_inst_0	61	45	0	0	0	0	0	0	0	0	0	0	0
packetization_inst_0	254	91	0	0	0	0	0	0	0	0	0	0	0
UART_interface_0	135	336	0	0	0	0	0	0	0	0	0	0	0
COREUART_C0_0	88	79	0	0	0	0	0	0	0	0	0	0	0
addr_decoder_V2_0	20	181	0	0	0	0	0	0	0	0	0	0	0
receive_data_v2_0	27	76	0	0	0	0	0	0	0	0	0	0	0
UART_TX_MUX_0	2	10	0	0	0	0	0	0	0	0	0	0	0
ident_coreinst	4312	4796	4536	4536	0	0	0	126	0	3	0	0	0
refclock_0	0	0	0	0	0	0	0	0	0	0	1	0	1

3.8 Ports (Ask a Question)

The following table lists the ports of the demo design.

Table 3-1. Input and Output Ports

Port Name	Direction	Description
RefClock		
REF_CLK_PAD_P_0 REF_CLK_PAD_N_0	Input	XCVR Reference clock 156.25 MHz
LANE0_TXD_N_0 LANE0_TXD_P_0	Output	XCVR serial data
JESD and Transceiver Peripheral Ports		
REF_CLK_PAD_P REF_CLK_PAD_N	Input	XCVR Reference clock input
DAC_SYNC_P DAC_SYNC_N	Input	Sync signal from AD9371
PADP PADN	Input	SYSREF signal from AD9371 FMC card

.....continued		
Port Name	**Direction**	**Description**
LANE3_RXD_N LANE3_RXD_P LANE2_RXD_N LANE2_RXD_P LANE1_RXD_N LANE1_RXD_P LANE0_RXD_N LANE0_RXD_P	Input	Transceiver lanes connected to AD9371
ADC_SYNC_P ADC_SYNC_N	Output	Sync signal to AD9371
LED_OUT	Output	Connected to LEDs on EVAL kit
LANE3_TXD_N LANE3_TXD_P LANE2_TXD_N LANE2_TXD_P LANE1_TXD_N LANE1_TXD_P LANE0_TXD_N LANE0_TXD_P	Output	Transceiver lanes connected to AD9371
MSS Peripheral Ports		
REF_CLK_0	Input	On Board 50 MHZ reference clock
TRSTB	Input	CoreJTAG pin
TCK	Input	CoreJTAG pin
TDI	Input	CoreJTAG pin
TMS	Input	CoreJTAG pin
SPI_SDI	Input	SPI Data input
TDO	Output	CoreJTAG pin
SPI_SCLK	Output	SPI Clock
SPI_SDO	Output	SPI Data out
SPI_SS0	Output	SPI chip select
SPI_SS1	Output	SPI chip select
GPIO_OUT	Output	GPIO[3] → reset JESD sub system GPIO[2] → UART MUX GPIO[4-9] → Connected to AD9371
UART Ports		
RX	Input	UART receiver for both UARTapb and CoreUART
TX	Output	UART transmitter for both UARTapb and CoreUART

4. Installing the Software Defined Radio Demo GUI (Ask a Question)

To install the Software Defined Radio demo GUI, perform the following steps:

1. Extract the contents of the `mpf_an5014_v2023p1_eval_df.zip` file and run the `setup.exe` file from `mpf_an5014_v2023p1_eval_df/GUI/Software_Defined_Radio_Demo_GUI_Installer/`.
2. Click **Yes** for any message from User Account Control. The Software Defined Radio demo GUI installation wizard is displayed.
3. Confirm the installation directory locations for the GUI and the National Instruments products and click **Next**.
4. Accept the license agreement and click **Next**.
5. Review the summary and click **Next**, then the installation proceeds with a progress bar. After the installation, a confirmation message is displayed.
6. Click **Next** to exit the installation wizard.
7. Restart the host PC when prompted. The Software Defined Radio demo GUI is installed.

5. Setting Up the Demo (Ask a Question)

The demonstration involves the following steps:

1. Setting up the hardware
   - For same board communication
   - For two boards communication
2. Programming the device

5.1 Setting Up the Hardware (Ask a Question)

After generating the bitstream, the PolarFire device is programmed on Evaluation kit by performing the following steps:

1. Ensure that the jumper settings on the board are same as listed in the following table.

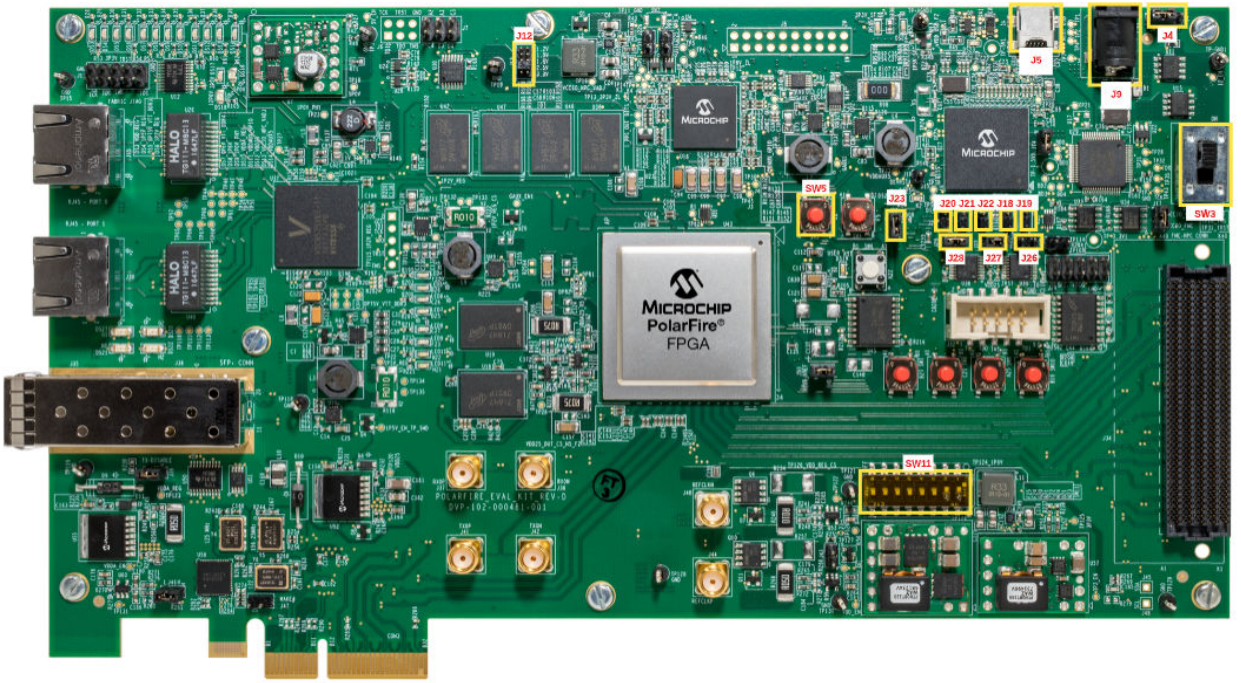
Table 5-1. Jumper Settings

Jumper	Description
J18, J19, J20, J21, J22	Close pin 2 and 3 for programming the PolarFire FPGA through FTDI
J28	Close pin 1 and 2 for programming through the on-board FlashPro5
J26	Close pin 1 and 2 for programming through the FTDI SPI
J27	Close pin 1 and 2 for programming through the FTDI SPI
J4	Close pin 1 and 2 for manual power switching using SW3
J12	Close pin 3 and 4 for 2.5 V
J23	Remain open
SW11	Switch 1 and 2. Selects Tx and Rx LO (Local Oscillator) frequency in AD9371. For more information, see 7. Changing the Tx and Rx frequency section.
SW5	Reset switch

2. Connect the power supply cable to the J9 connector on the board.
3. Connect the USB cable from the host PC to the J5 (FTDI port) on the board.
4. Power on the board using the SW3 slide switch.
5. For external loop back demo, connect TX1 to RX1 using the 1 SMA to SMA cables.

The following figure shows the board setup for the mentioned jumper settings.

Figure 5-1. PolarFire FPGA Evaluation Kit Jumper Settings for SDR



When the board is powered up, power supply LEDs DS3 to DS14 is switched on. For more information about LEDs on the PolarFire FPGA Evaluation Kit, see UG0747: PolarFire FPGA Evaluation Kit User Guide.

5.1.1 Same Board Communication (Ask a Question)

To setup same board communication, perform the following steps:

1. Connect the AD9371 with the FMC Connector of the PolarFire FPGA Evaluation kit.
2. Connect the SMA antenna at the transmitter and other SMA antenna at the receiver part as shown in the Figure 7-2.
3. Ensure that the jumper setting are as per the Table 5-1 and power up the board.

5.1.2 Two Boards Communication (Ask a Question)

To setup two boards communication, perform the following steps:

1. Connect the AD9371 with the FMC Connector of the PolarFire FPGA Evaluation kit and follow the same for the other board.
2. Connect the SMA antenna at the Transmitter of board 1 and connect the other antenna at the receiver of the board 2 as shown in Figure 7-1.
3. Ensure that the jumper settings are as per the Table 5-1, and the board is powered up and the same must be done with the second board.

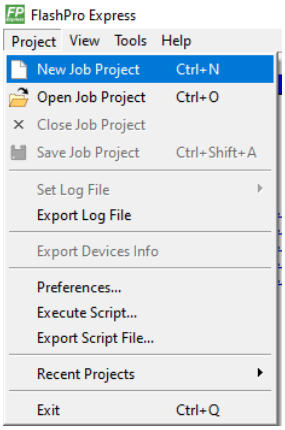
5.2 Programming the Device (Ask a Question)

This section describes how to program the PolarFire FPGA Evaluation kit with the job file using FlashPro Express. To program the device, perform the following steps:

The `PFEval_SDR.job` file is available at `mpf_an5014_v2023p1_eval_df\Programming_File`.

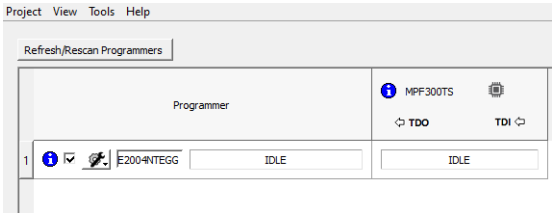
1. Connect a micro USB to **J5** from the host PC and start the FlashPro Express software from its installation.
2. Select **New** or **New Job Project** from the Project menu to create a new job project, as shown in the following figure.

Figure 5-2. FlashPro Express Job Project



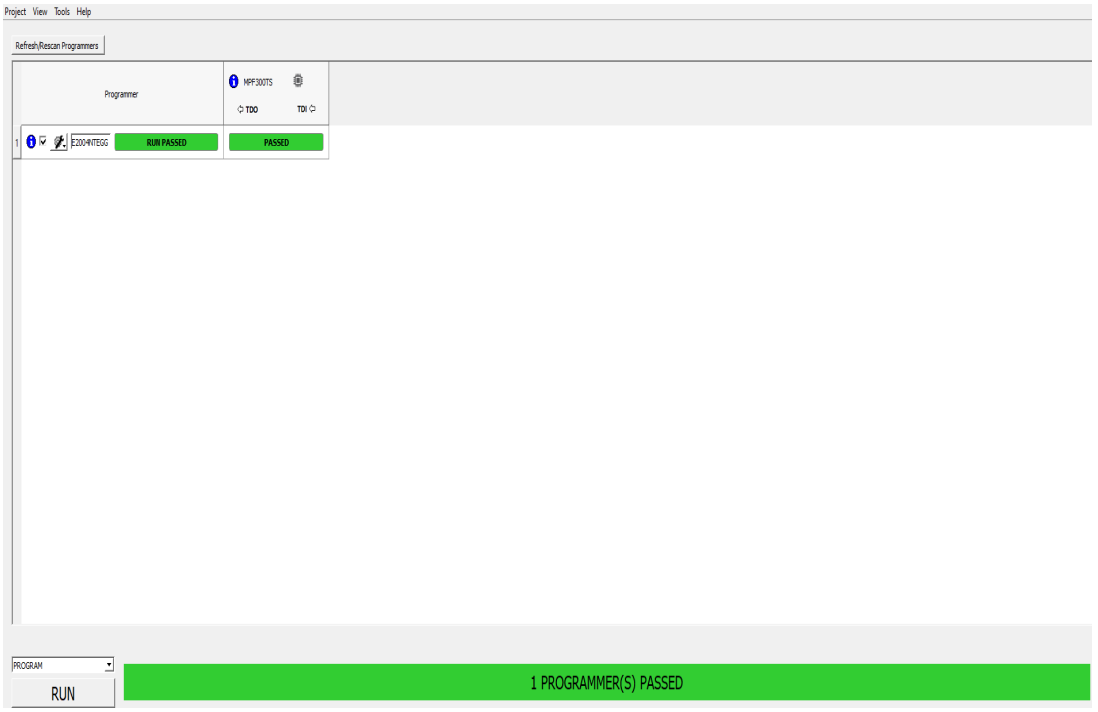
3. In the **FlashPro Express Job** dialog box, enter the following values in the New Job Project:
   - **Programming job file**: Click **Browse**, and navigate to the location where the `.job` file is located and select the file. The default location is: `<$download_directory>\mpf_an5014_v2023p1_eval_df\Programming_File`.
   - **FlashPro Express job project location**: Click **Browse**, and navigate to the location where you want to save the project.
4. Click **OK**. The required programming file is selected and ready to be programmed in the device.
5. The FlashPro Express window appears as shown in the following figure. Confirm that a programmer number (for example, 79DE6C53) appears in the Programmer field. If it does not, then confirm the board connections and click **Refresh/Rescan Programmers**.

Figure 5-3. Programming the Device



6. Click **RUN**. When the device is programmed successfully, a **RUN PASSED** status is displayed as shown in the following figure.

Figure 5-4. FlashPro Express—RUN PASSED



7. Close **FlashPro Express** or in the Project tab, click **Exit**.
8. Power cycle the board using **SW5**.

6. SoftConsole (Ask a Question)

The softconsole project included with the Libero design, uses the APIs for AD9371 and AD9528 from analog devices which are used to initialize and configure the clock generator AD9528. The RF transceiver AD9371 which has a built in ARM processor that runs calibration and other power up sequences required to initialize AD9371. The ARM binary byte file required for the built in ARM processor is loaded by the soft Mi-V processor in the FPGA power up sequence, which indeed communicates with AD9371 and AD9528 by Serial Peripheral Interface (SPI). The Mi-V processor reads the status of AD9528 and AD9371 through SPI during initialization and displays the status on UART terminal.

The following listed messages are displayed on the **Receive Data** window:

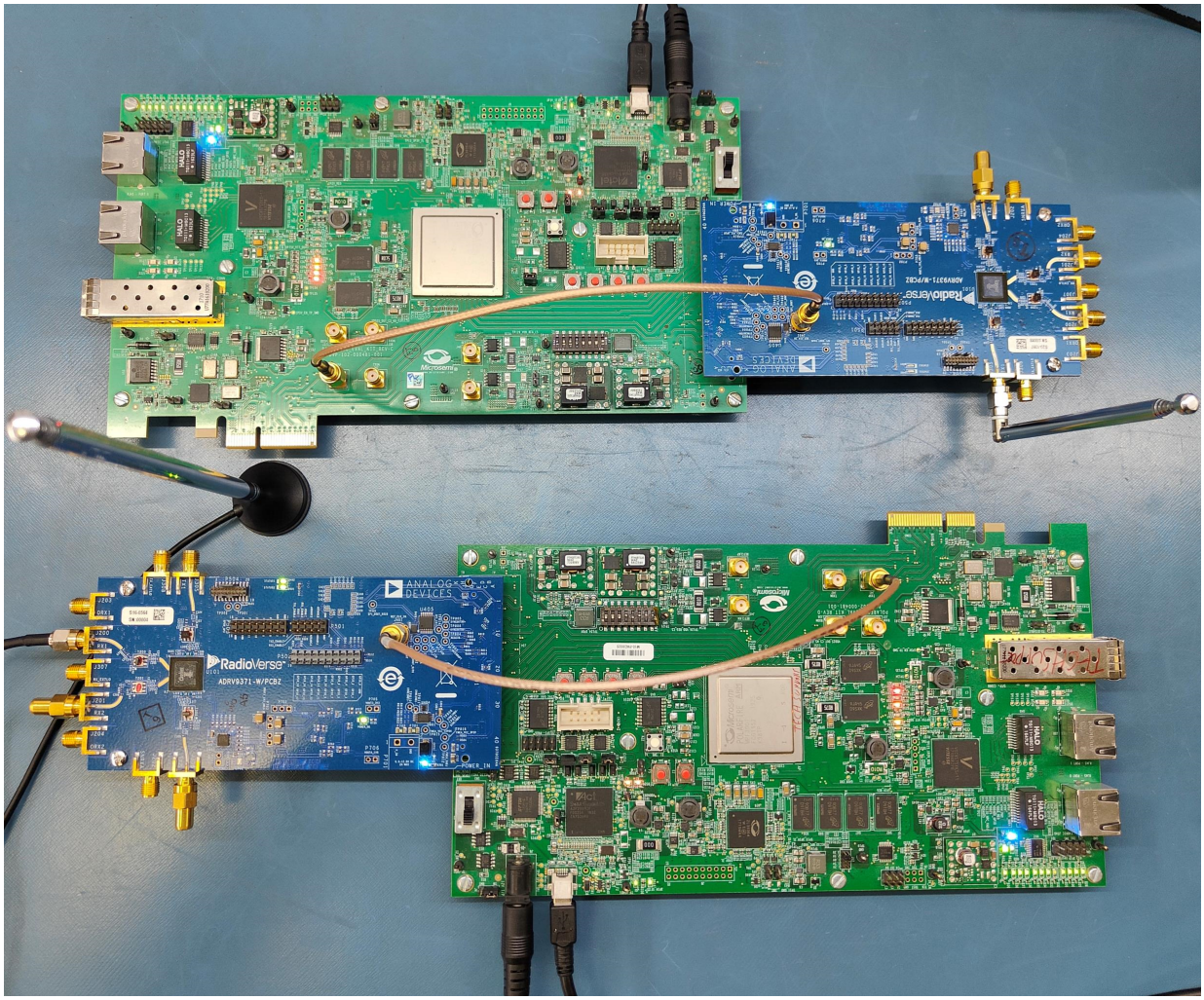
- **SPI AD9371**: Before the SPI communication in the Mi-V processor with AD9371 (and AD9528) is initiated, it is displayed on the screen only after the appropriate UART initialization. If this message is not displayed or some random data is displayed on the GUI, then check the UART baudrate value in the GUI.
- **PLL Locked**: The Mi-V processor checks the status of the CLKPLLL bit and when CLKPLL is locked, this message is displayed. If not locked, then **PLL not locked** is displayed.
- **Multi Chip Sync Successful**: After performing Multi Chip Sync, the Mi-V processor verifies if the Multi Chip Sync is successful or not. This message is displayed if it is successful. If not, then **Multi Chip Sync Failed** is displayed.
- **AD9371 ARM Version 4.0.6**: After loading an ARM binary byte file, the Mi-V processor reads back the version of the binary just loaded by it. This message is displayed if binary byte array is properly loaded and the version is read back. If not loaded properly, then an arbitrary number is displayed.
- **(CLK, RX, TX, SNIFFER) PLLs Locked**: This message is displayed when the Mi-V processor checks for the PLL locks for CLK, RX, TX, and sniffer. If not locked, it displays the message (CLK, RX, TX, SNIFFER) PLLs not locked along with PLL lock status. For more information about PLL status bits, see the UG992 AD9371 user guide for analog devices.
- **Calibrations Completed Successfully**: The Mi-V processor queries the calibration status of AD9371. This message is displayed if the ARM processor (in the AD9371) successfully completes calibrations. Otherwise, this message is not displayed.
- **Successfully Initialised AD9371**: This is the final message. It is displayed when AD9371 is initialized and configured correctly. If AD9371 is not configured correctly or it fails to initialize, then the message **Initialization Failed, Status =XXXX**, is displayed along with the status bits (indicated as XXXX). The status bits are used to debug failures during initialization.

7. Running the Demo (Ask a Question)

To execute the demo, perform the following steps:

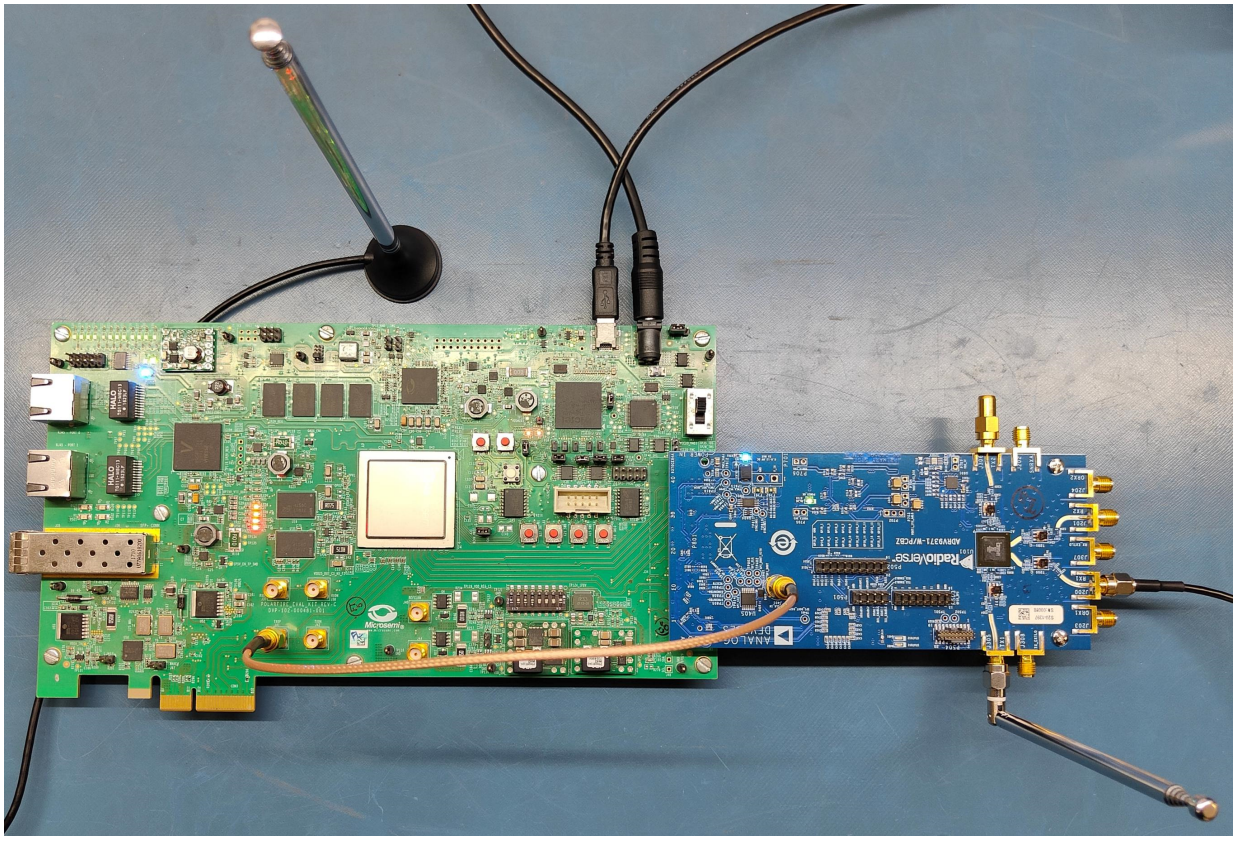
1. After programming the PolarFire FPGA Evaluation kit, connect AD9371 to the FMC connector.
2. Connect the SMA cable to the J41 pin on the PolarFire FPGA Evaluation kit and J401 on the AD9371. This acts as the reference clock to the FMC card.
3. Depending on the type of the demo being used, connect the antennas to the respective transmitter and receiver of the FMC card. if demo is running on two boards, connect one antenna to J305 (Tx1) of the first demo kit and connect second antenna to J200 (Rx1) of the second demo kit.

Figure 7-1. Setting Up of Two PolarFire Evaluation Kit with AD9371



4. For running the demo on the same board, connect one antenna to J305 (Tx1) and second antenna to the J200 (Rx1) of the same board.

Figure 7-2. Setting Up of PolarFire Evaluation Kit with AD9371



This SDR demo features the transmit and receive the data or image in the wireless medium. The data is transmitted through UART from GUI to the transmitter, then the data sent is packed, encoded, and modulated. The final modulated data is transmitted over the air and received at the receiver end.

Changing the Tx and Rx frequency

SDR demo runs in four different LO frequencies. Use the DIP switch SW11 to modify the LO frequency – ensure to configure the same frequency on the transmit and receive sides. In the two-board demonstration, the distance between the antennas is determined by the configured frequency. The following table lists the available LO frequencies.

Table 7-1. Frequency Settings

Switch [2:1]	LO Frequency
ON : ON	700 MHz
ON : OFF	1200 MHz
OFF : ON	2400 MHz
OFF : OFF	5800 MHz

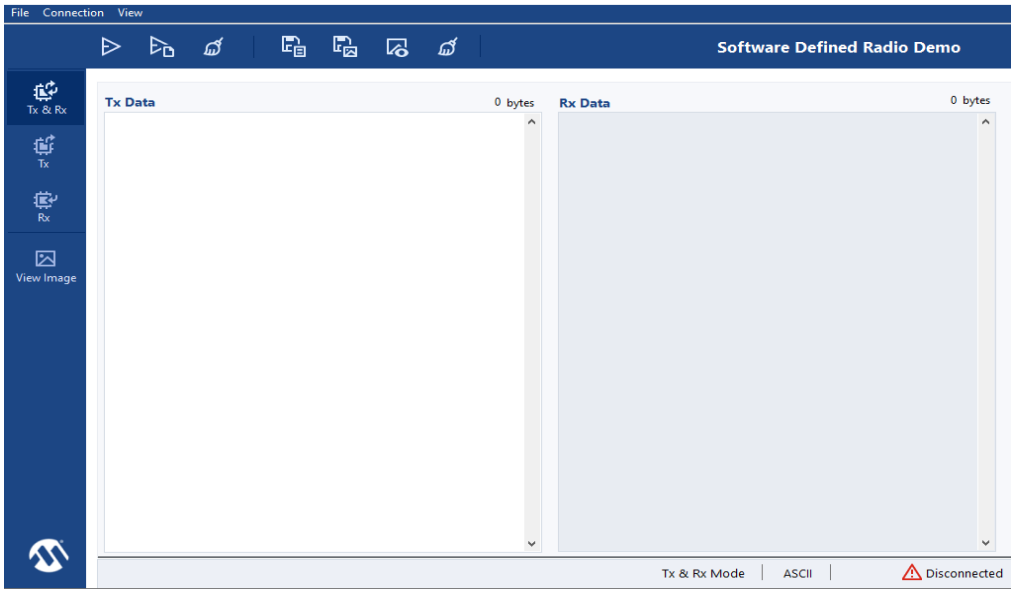
Important: Make sure to toggle reset (SW5) after changing the LO Frequency.

7.1 Running the Demo on Same Board (Ask a Question)

To run demo on same board, perform the following steps:

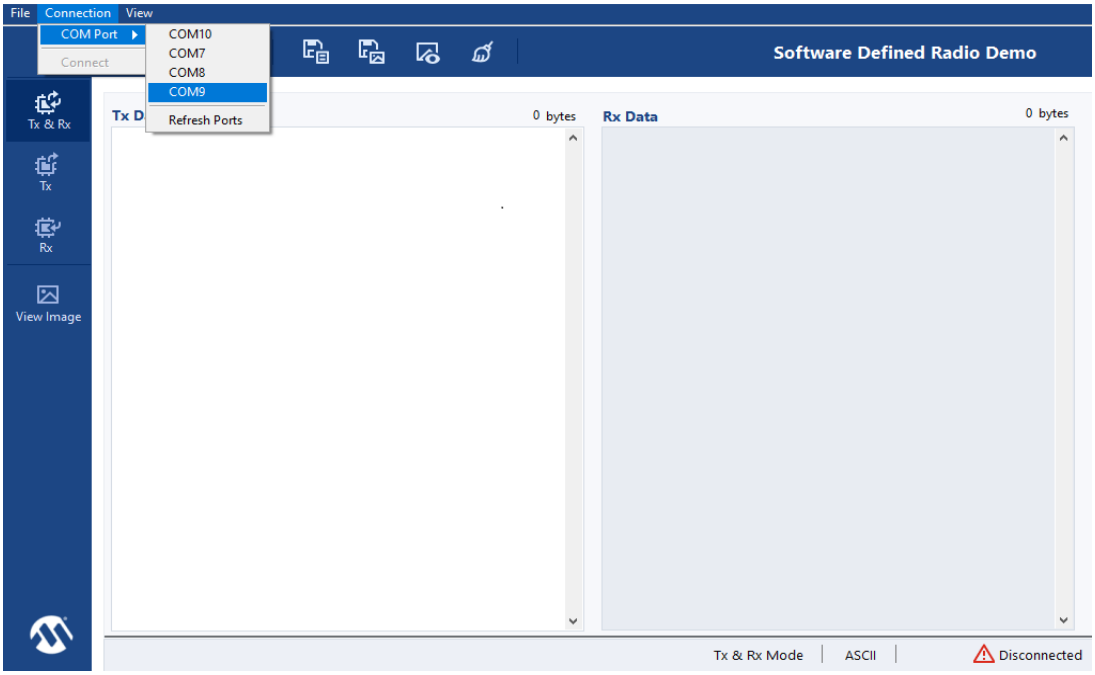
1. After programming the bit files, launch the GUI, see the following figure.

Figure 7-3. Displayed GUI



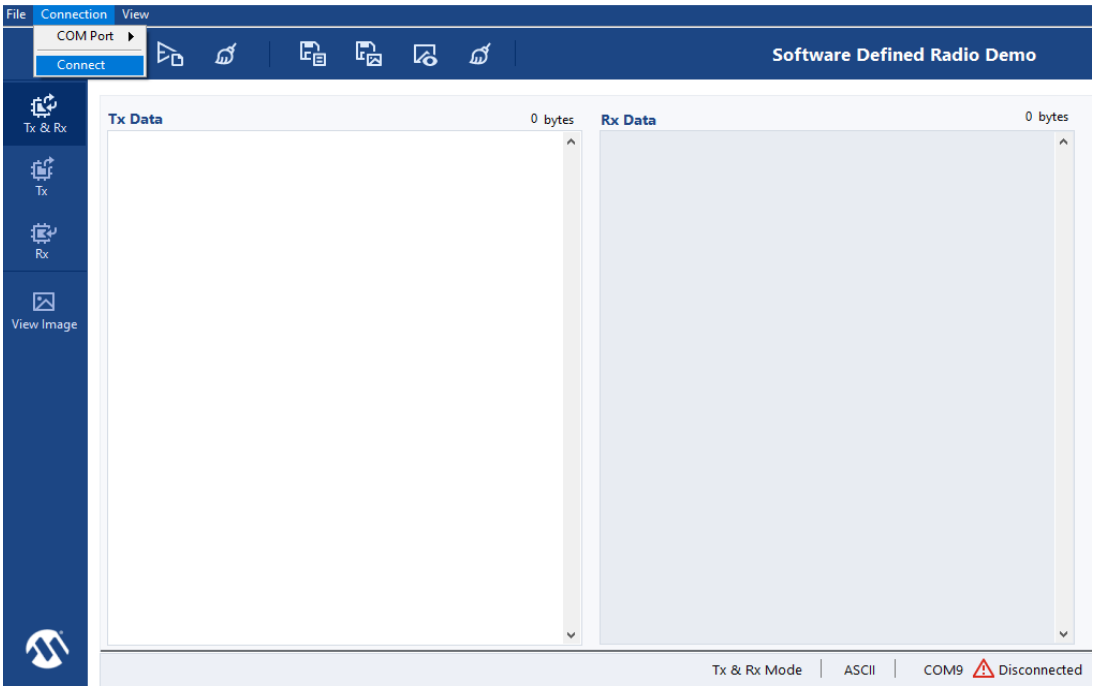
2. On the **Connection** tab, point to COM Port, click **Refresh Ports** and then click the appropriate (3rd port corresponding to Flashpro - COM9) **COM Port** connected to the PC.

Figure 7-4. Com Port Connection



3. On the **Connection** tab, click **Connect**.

Figure 7-5. Connection Establishment

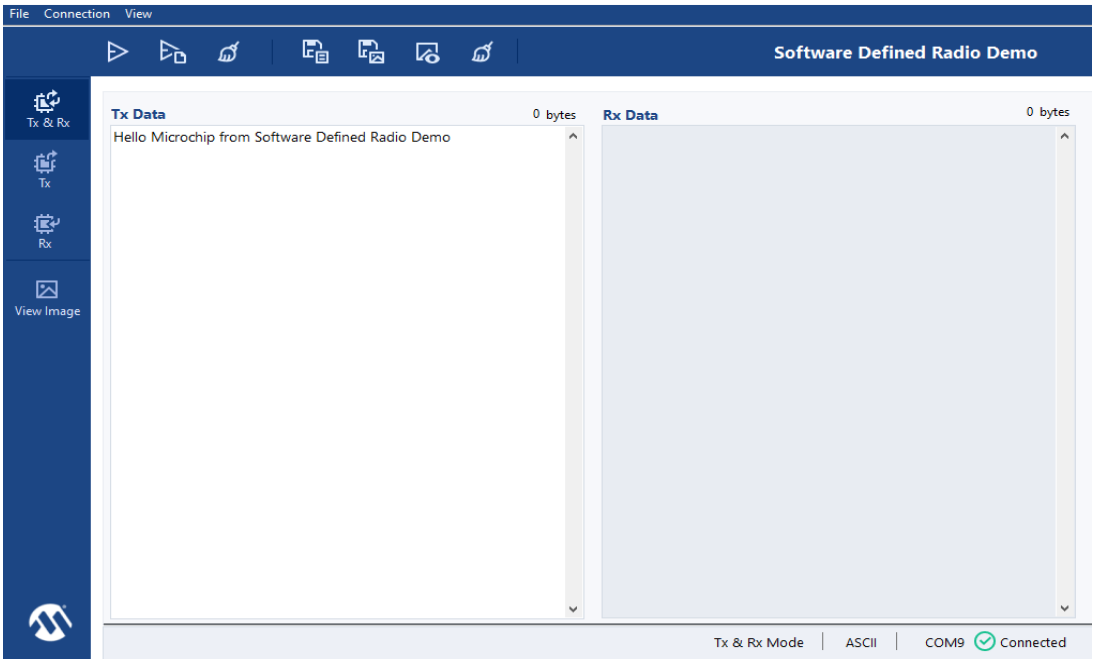


4. Check for the connection status at right bottom corner of the GUI.

Figure 7-6. Connection Status

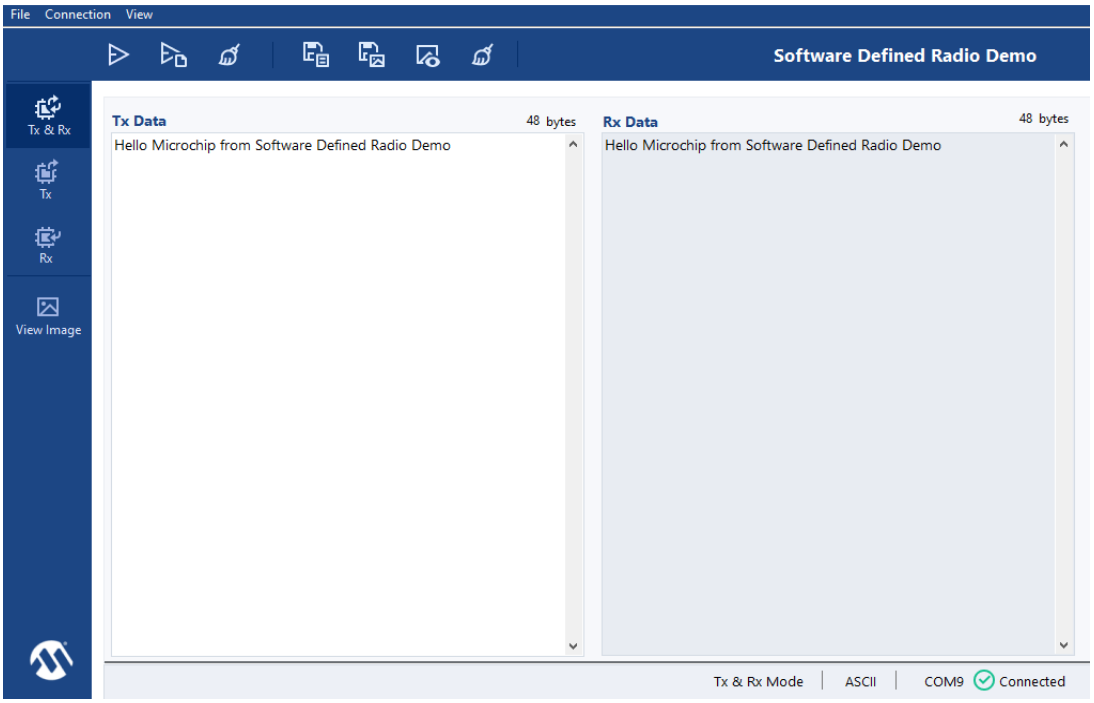
5. After successful connection, setup is ready for the wireless transfer of data. In the **Tx Data** box, type text data and click  .

Figure 7-7. Data Sent from Transmitter Side



6. After successful transfer, the received data must appear in the **Rx Data** box.

Figure 7-8. Data Received at Receiver Side



7.2 Running the Demo on Two Boards (Ask a Question)

To run demo on two boards, perform the following steps:

1. Place the Transmitter (Tx) and Receiver (Rx) antennas with in 1 meter range. The range limitation is due to the limited RF gain of AD9371. The range is extended by using a RF amplifier at transmitter output.
2. After programming the bit files, launch the GUI in the PC where Transmitter antenna is connected.
3. Select the appropriate port for the communication in **Connection** tab and click **Connect**.
4. Check for the connection status at right bottom corner of the GUI.

Figure 7-9. Connection Status

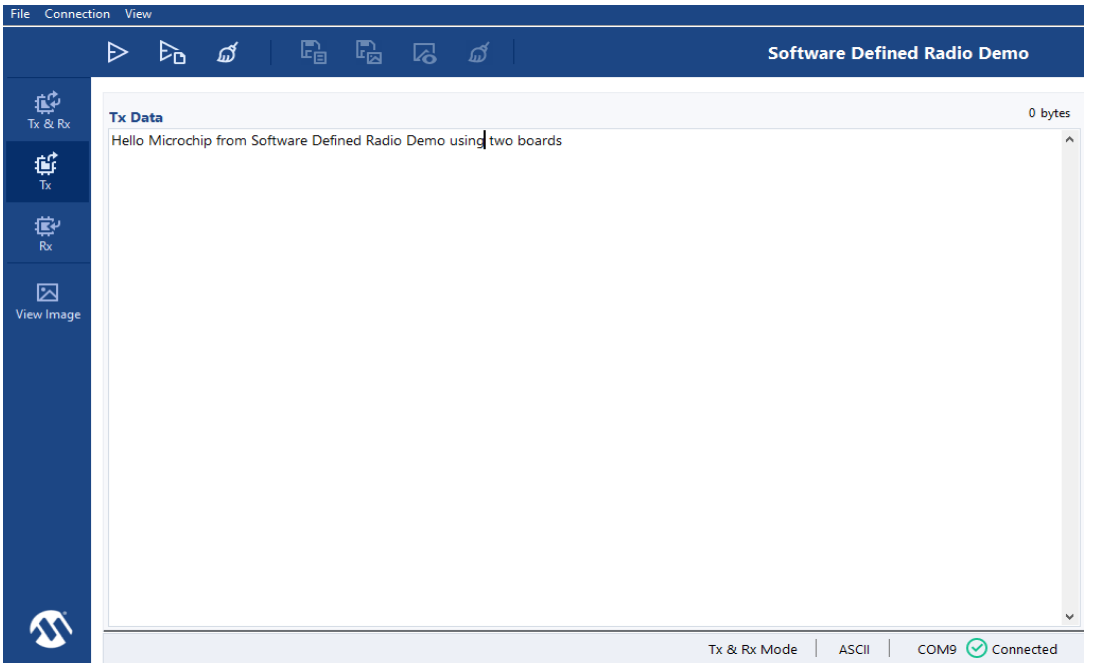
5. By this, point connection is established and GUI is ready to send or receive the data.
6. Repeat the same steps for the PC connected to the Receiver antenna.
7. You can send data in the following two ways:

   a. Enter data and click **Send**  .

   b. Click **Send from File**  .

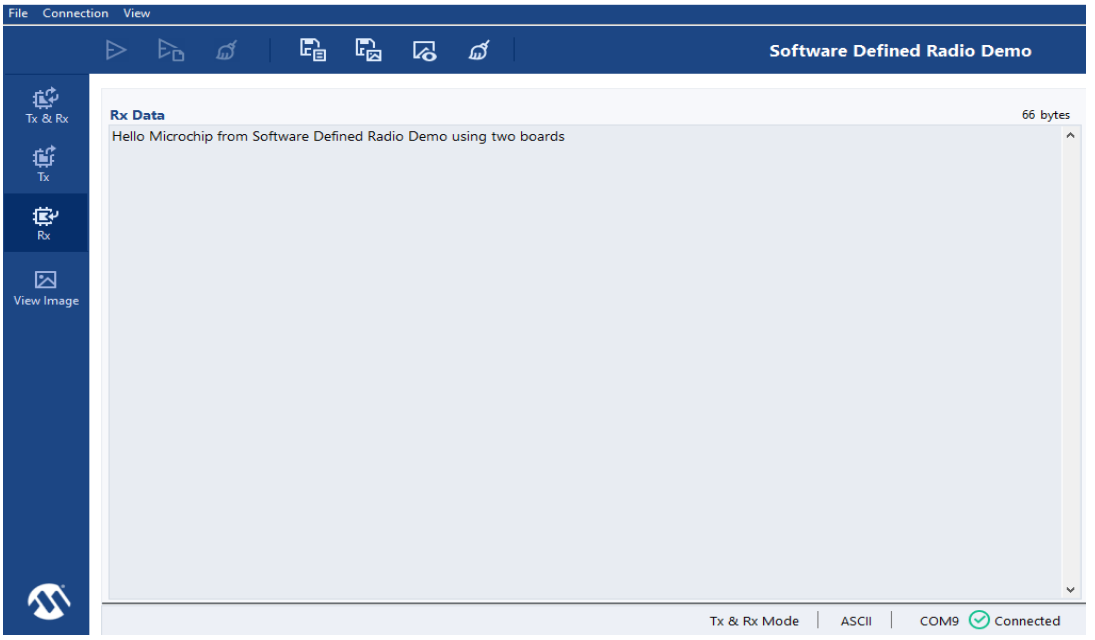
   The following figure is an example where data is sent by clicking Send.

Figure 7-10. Data Sent from Transmitter Side



8. After data is entered, click **Send** .
9. After a successful transfer, the message is displayed on the receive data window on the GUI connected to the RX antenna.

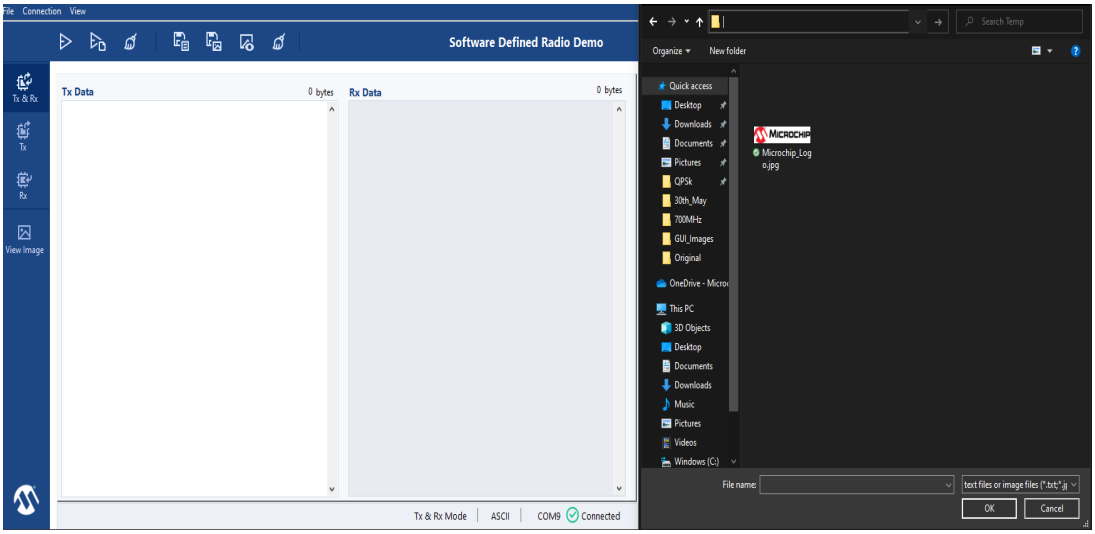
Figure 7-11. Data Received at Receiver Side



SDR demo also supports sending `.jpg` image. To transfer image, perform the following steps:

1. Click on **Send file** , select the `.jpg` file through the popup browser window and click **Send** .

Figure 7-12. File Selection



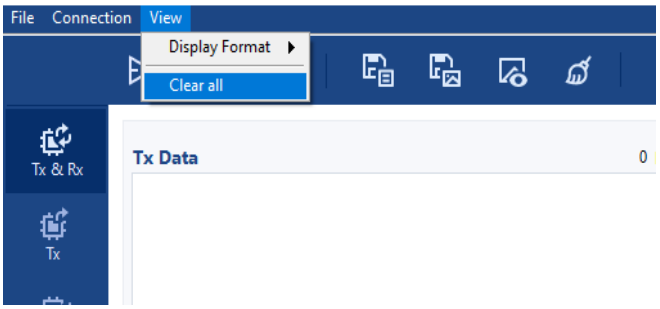
2. After successful transfer of the image, to see the received image, click **View image** 

.

Figure 7-13. After Successful Transfer

3. After successful image reception at Rx, on the **View** tab, click **Clear all** before sending the next data/image.

Figure 7-14. Clear Data for Sending Next Data/Image



8. Revision History (Ask a Question)

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Table 8-1. Revision History

Revision	Date	Description
1	06/2023	Initial release

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